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MTTL

INTEGRATED CIRCUITS
MC500/MC400 SERIES

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MTTL

INTEGRATED CIRCUITS

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NUMERICAL INDEX (Functions and Characteristics)

V_{CC} = 5.0 V, T_A = 25°C

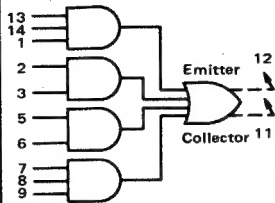
Function	Type		Output Loading Factor Each Output		Propagation Delay t_{pd} ns typ	Power Dissipation mW typ/pkg	Page No.
	Case 609, 93 0 to +75°C	Case 609 -55 to +125°C	MC400 Series	MC500 Series			
Dual 4-Input NAND Gate	MC400 MC450	MC500 MC550	12 6	15 7	10	30	4-14
Expandable 4-Wide 2-2-2-3-Input AND-OR-INVERT Gate	MC401 MC451	MC501 MC551	12 6	15 7	12	30	4-24
Single 8-Input NAND Gate	MC402 MC452	MC502 MC552	12 6	15 7	12	15	4-10
2-Wide 3-Input AND-OR-INVERT Gate with Gated Complement	MC403 MC453	MC503 MC553	12 6	15 7	11	35	4-27
Expandable 3-Wide 3-Input AND-OR-INVERT Gate	MC404 MC454	MC504 MC554	12 6	15 7	12	25	4-20
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AND J-K Flip-Flop	MC415 MC465	MC515 MC565	12 6	15 7	f = 20 MHz	40	4-32
OR J-K Flip-Flop	MC416 MC466	MC516 MC566	12 6	15 7	f = 20 MHz	50	4-37
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GATES

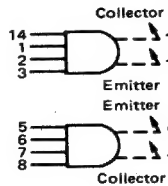
<p>MC400/MC450 MC500/MC550 Dual 4-Input NAND Gate</p> <p>$12 = \overline{1 \cdot 2 \cdot 3 \cdot 4}$</p> <p>$t_{pd} = 10 \text{ ns typ}$ $P_D = 30 \text{ mW typ/pkg}$</p>	<p>MC401/MC451 MC501/MC551 Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate</p> <p>$12 = \overline{(1 \cdot 2) \cdot (3 \cdot 4) \cdot (5 \cdot 6) \cdot (7 \cdot 8) \cdot (9 \cdot 10 \cdot 11)}$</p> <p>$t_{pd} = 12 \text{ ns typ}$ $P_D = 30 \text{ mW typ/pkg}$</p>	<p>MC403/MC453 MC503/MC553 2-Wide 3-Input AND-OR-INVERT Gate with Gated Complement</p> <p>$12 = \overline{(1 \cdot 2 \cdot 3) \cdot (4 \cdot 5 \cdot 6) \cdot (7 \cdot 8)}$</p> <p>$t_{pd} = 11 \text{ ns typ}$ $P_D = 35 \text{ mW typ/pkg}$</p>
<p>MC402/MC452 MC502/MC552 Single 8-Input NAND Gate</p> <p>$12 = \overline{1 \cdot 2 \cdot 3 \cdot 4 \cdot 5 \cdot 6 \cdot 7 \cdot 8}$</p> <p>$t_{pd} = 12 \text{ ns typ}$ $P_D = 15 \text{ mW typ/pkg}$</p>	<p>MC404/MC454 MC504/MC554 Expandable 3-Wide 3-Input AND-OR-INVERT Gate</p> <p>$12 = \overline{(1 \cdot 2 \cdot 3) \cdot (4 \cdot 5 \cdot 6) \cdot (7 \cdot 8 \cdot 9) \cdot (10 \cdot 11 \cdot 12)}$</p> <p>$t_{pd} = 12 \text{ ns typ}$ $P_D = 25 \text{ mW typ/pkg}$</p>	<p>MC406/MC456 MC506/MC556 Expandable 8-Input NAND Gate</p> <p>$12 = \overline{1 \cdot 2 \cdot 3 \cdot 4 \cdot 5 \cdot 6 \cdot 7 \cdot 8}$</p> <p>$t_{pd} = 18 \text{ ns typ}$ $P_D = 15 \text{ mW typ/pkg}$</p>
<p>MC408/MC458 MC508/MC558 Quad 2-Input NAND Gate</p> <p>$3 = \overline{1 \cdot 2}$</p> <p>$t_{pd} = 10 \text{ ns typ}$ $P_D = 60 \text{ mW typ/pkg}$</p>	<p>MC412/MC462 MC512/MC562 Triple 3-Input NAND Gate</p> <p>$5 = \overline{1 \cdot 2 \cdot 3}$</p> <p>$t_{pd} = 10 \text{ ns typ}$ $P_D = 45 \text{ mW typ/pkg}$</p>	<p>MC420/MC470 MC520/MC570 Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate</p> <p>$12 = \overline{(1 \cdot 2) \cdot (3 \cdot 4) \cdot (5 \cdot 6)}$</p> <p>$t_{pd} = 12 \text{ ns typ}$ $P_D = 40 \text{ mW typ/pkg}$</p>

EXPANDERS

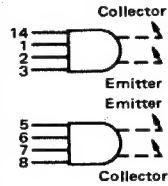
MC409/MC459
MC509/MC559
4-Wide 3-2-2-3 Input Expander
for AND-OR-INVERT Gates



MC410/MC460
MC510/MC560
Dual 4-Input Expander
for AND-OR-INVERT Gates

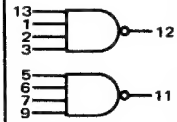


MC411/MC461
MC511/MC561
Dual 4-Input Expander
for NAND Gates



DRIVER

MC407/MC457
MC507/MC557
Dual 4-Input
Line Driver

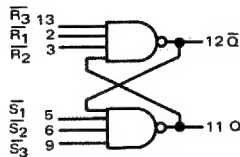


$$12 = 1 \cdot 2 \cdot 3 \cdot 13$$

$t_{pd} = 25 \text{ ns typ}$
@ 1000 pF Load
 $P_D = 60 \text{ mW typ/pkg}$

FLIP-FLOPS

MC413/MC463
MC513/MC563
R-S Flip-Flop

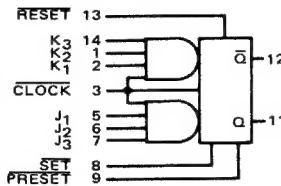


\bar{R}	\bar{S}	Q_{n+1}	\bar{Q}_{n+1}
0	0	Not allowed	1
0	1	0	1
1	0	1	0
1	1	Q_n	\bar{Q}_n

Where $\bar{R} = \bar{R}_1 \cdot \bar{R}_2 \cdot \bar{R}_3$
 $\bar{S} = \bar{S}_1 \cdot \bar{S}_2 \cdot \bar{S}_3$

$f = 20 \text{ MHz}$
 $P_D = 30 \text{ mW}$

MC415/MC465
MC515/MC565
AND J-K Flip-Flop

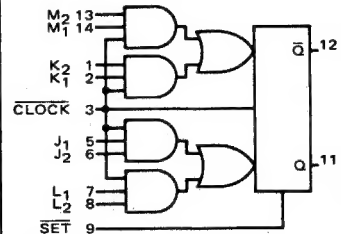


J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	0	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Where $J = J_1 \cdot J_2 \cdot J_3$
 $K = K_1 \cdot K_2 \cdot K_3$

$f = 20 \text{ MHz}$
 $P_D = 40 \text{ mW}$

MC416/MC466
MC516/MC566
OR J-K Flip-Flop



J	L	K	M	Q_n	Q_{n+1}
0	0	X	X	0	0
1	X	X	X	0	1
X	1	X	X	0	1
X	X	0	X	1	1
X	X	1	X	1	0
X	X	X	1	1	0

X = Don't Care

Where $J = J_1 \cdot J_2$
 $L = L_1 \cdot L_2$
 $K = K_1 \cdot K_2$
 $M = M_1 \cdot M_2$

$f = 20 \text{ MHz}$
 $P_D = 50 \text{ mW}$

MTTL

GENERAL INFORMATION SECTION

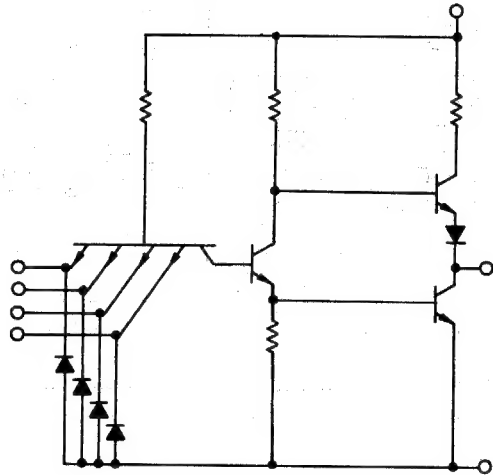
INTRODUCTION

MTTL transistor-transistor logic is a medium speed, high-noise-immunity family of saturating integrated logic circuits.

The circuits in the MTTL family are identified by a multiple emitter input transistor and an active "pull-up" in the upper output network as shown in Figure 1.

The multiple emitter input configuration offers the maximum amount of logic capability in the minimum physical area and provides improved switching characteristics during turnoff. Clamp diodes are provided at each of the inputs to limit undershoot that occurs in typical system applications such as driving long interconnect wiring. The active pull-up output configuration provides low impedance in the high output state. The resulting low impedances in both states provide excellent ac noise immunity and allow high-speed operation while driving large capacitive loads.

FIGURE 1 – TYPICAL MTTL CIRCUIT



MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage — Continuous MC500 Series MC400 Series	+8.0 +7.0	Vdc
Supply Operating Voltage Range	4.5 to 6.0	Vdc
Input Voltage	+5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range MC500 Series MC400 Series	-55 to +125 0 to +75	°C
Storage Temperature Range Flat Package Plastic Package	-65 to +200 -55 to +125	°C
Maximum Junction Temperature MC500/550 Series MC400/450 Series	+175 +150	°C
Thermal Resistance - Junction To Case (θ_{JC}) Ceramic Flat Package Plastic Dual-In-Line	0.09 0.15	°C/mW
Thermal Resistance - Junction To Ambient (θ_{JA}) Ceramic Flat Package Plastic Dual-In-Line	0.26 0.30	°C/mW

TYPICAL CHARACTERISTICS

The following summary presents the typical operating characteristics of the MTTL family. Unless otherwise indicated, the parameters are defined for $V_{CC} = +5.0$ volts and $T_A = +25^\circ\text{C}$.

Supply Voltage Operating Range = 4.5 to 6.0 volts

Operating Temperature Range:

MC500/550 Series = -55 to $+125^\circ\text{C}$

MC400/450 Series = 0 to $+75^\circ\text{C}$

Output Drive Capability

Other Gates (Output Loading Factor):

MC500 Series = 15 MC500 or MC550 Series Gates.

MC550 Series = 7 MC500 or MC550 Series Gates.

MC400 Series = 12 MC400 or MC450 Series Gates.

MC450 Series = 6 MC400 or MC450 Series Gates.

Capacitance = 600 pF

Output Impedance

High State = 70 ohms (unsaturated) nominal

Low State = 10 ohms nominal

Output Voltage Swing = 0.2 to 3.5 volts typical

Input Voltage Limits

+5.5 volts maximum

-0.5 volt minimum

Switching Threshold = 1.5 volts nominal

Input Impedance

High State = 400 k ohms nominal

Low State = 4.0 k ohms nominal

Worst-Case DC Noise Margin

High State - MC500/550 series 0.700 volt minimum

MC400/450 series 0.600 volt minimum

Low State - MC500/550 series 0.750 volt minimum

MC400/450 series 0.750 volt minimum

Power Dissipation

15 mW per gate typical

40-50 mW per flip-flop typical

Switching Speeds⁽¹⁾

Average Propagation Delay = 10 ns per gate typical

18 ns per flip-flop typical

Rise Time = 2.5 ns typical

Fall Time = 1.5 ns typical

Flip-Flop Clock Frequency (MC515/516 Series) = 20 MHz maximum.

BREADBOARDING SUGGESTIONS

When breadboarding with any form of high-speed, high-performance TTL, the designer must continually be aware of the fact that he is working with the fastest form of saturating logic available in the industry today. The switching speeds, especially the frequencies associated with the very fast rise and fall times of the circuits, are in the RF range and good high-frequency layout techniques should be used. The following breadboarding suggestions have been included to help the designer in his initial circuit layout. In many cases the breadboarding suggestions will have to be modified to meet the requirements of the designer's specific application.

Power and Ground Distribution

Special care should be taken to insure adequate distribution of power and ground systems. The typical rate of change of currents and voltages for a single MTTL gate is in the range of 10^7 A/s and 10^8 V/s respectively. These figures reflect the necessity for a low-impedance power supply and ground distribution system, if transients are to be minimized and noise margins maintained. The use of AWG No. 20 wire or larger is often required. For printed circuitry, line widths of 100 mils or more are often necessary. A ground plane is desirable when using a large number of units.

Bypassing

To reduce supply transients, the breadboard should be bypassed at the point where power is supplied to the board and at intervals throughout the board. The use of a single bypass capacitor at the output terminal of the power supply is not adequate in a breadboard utilizing the fast rise and fall time MTTL circuits. A comparatively large, low-inductance type capacitor (in the $1.0\ \mu\text{F}$ range) is suggested at the point where power and ground enter the board. In many cases it has been found that distributing $0.01\ \mu\text{F}$ capacitors for every eight packages throughout a breadboard is adequate to suppress normal switching transients. It is also suggested that a bypass capacitor be placed in close proximity to any circuit driving a large capacitive load.

Power Dissipation

The standard supply voltage of the MTTL logic circuits is +5.0 Vdc. The typical average dc power dissipation is given for each MTTL circuit.⁽²⁾ It should be noted that the totem pole output common to all high level MTTL circuits has an associated ac power dissipation factor. This factor results from the timing overlap of the upper and lower output transistors during the normal switching operation and is typically 0.35 mW/MHz/output for a 15 pF load. This ac power dissipation should be added when calculating the total power requirements of the MTTL circuits.

Unused Inputs and Unused Gates

The unused inputs of any MTTL logic circuit should not be left open, and can either be tied to the used inputs or returned to the supply voltage. This will reduce any potential problems resulting from external noise. If the inputs are returned to the supply voltage, care should be taken to insure that the supply voltage does not exceed the maximum rated input voltage of 5.5 volts. If the supply can exceed 5.5 volts, the unused inputs must be returned to a lower voltage. The total number of inputs that can be tied to the output of any driving gate is 50. (This is defined as high state output loading factor.) It should be noted that the low state output loading rules must still be maintained. The minimum logical "1" level for the high state output loading is summarized for $V_{CC} = 5.0\ \text{V}$, $V_{IL} = 0.45\ \text{V}$ and $I_{OH} = -5.0\ \text{mA}$:

MC500/550 Series - $V_{OH} = 2.8$ volts minimum @ -55°C

MC400/450 Series - $V_{OH} = 3.0$ volts minimum @ 0°C

The unused inputs of the various flip-flops may be tied back to their associated outputs. To determine which outputs are related to each set of inputs by internal feedback, refer to the circuit schematics.

The inputs of any unused gate in a package should be grounded. This places the gate in its lowest power condition and will help to eliminate unnecessary power drain.

Expanders and Expander Nodes

The ORing nodes of all the M TTL AND-OR-INVERT gates are made available for expanding the number of AND gates to 10. Since these are comparatively high-impedance nodes, care should be taken to minimize capacitive loading on the expander terminals if switching speed is to be maintained. When an expander is to be used with an expandable AND-OR-INVERT gate, it should be placed as close as possible to the gate being expanded. The increase in the average propagation delay per AND gate added to an expandable AND-OR-INVERT gate is typically 1.0 ns/AND gate. The increase in average propagation delay as a function of capacitance added to the expander nodes is typically 1.0 ns/pF.

Output OR (AND) Function

Unlike the M TTL family of logic circuits, the outputs of the M TTL logic circuits cannot be tied together to perform the output OR, or more correctly, the output AND function. If the outputs of the M TTL family devices are tied together, it would be possible for the lower output transistor of one circuit and the upper output transistor of another circuit to be "on" simultaneously. This condition provides a low-impedance path from V_{CC} to ground and the current that flows (approximately I_{SC}) exceeds the guaranteed sink current. As a result, the saturated state cannot be maintained and the desired logic function is not satisfied.

Operating Characteristics of Flip-Flops

The general operating characteristics and restrictions for the MC515/MC516 series J-K flip-flops are as follows:

The clocked inputs are inhibited when the clock is in the low state, and data should be applied and allowed to settle. The clocked inputs are enabled when the clock goes high and data enters the flip-flop. The data is temporarily stored in the charge-storage section (temporary memory) while the clock is in the high state. This data is transferred to the bistable section on the negative clock transition.

The data on the clocked inputs should not be changed while the clock is in the high state. Data changes during this clock condition require 300 ns settling time.

The direct SET, PRESET, and RESET inputs do not directly affect the charge-storage section and therefore should not be used while the clock is high. On the negative transition of the clock, previously stored data may override the asynchronous set output state. Further, the direct SET, PRESET, and RESET inputs do not

MTTL

GENERAL INFORMATION SECTION

override the clock and will not control the state of the flip-flop until 120 ns after the negative transition of the clock. The clock signal must conform to the following boundary conditions at +125°C.

Maximum guaranteed clock frequency	= 20 MHz
Maximum clock fall time	= 150 ns
Minimum clock pulse width	= 20 ns
Minimum clock pulse amplitude	= 1.8 V
Maximum negative clock voltage	= -0.5 V

Note: These boundary conditions for operation are not defined as occurring simultaneously.

The transfer of data from the charge storage section to the bistable section is essentially an ac operation and thus results in the restriction of the clock fall time. If the clock fall time is greater than 150 ns, the information retained in the charge-storage section may not be transferred to the bistable section. The flip-flop will operate from very low frequencies to 20 MHz as long as the clock fall time is less than or equal to 150 ns.

Large negative clock excursions may cause incorrect data transfers to the bistable section during the transfer cycles. Therefore, the most negative clock signal should be limited to -0.5 volt.

(1) The switching characteristics of the M TTL family are defined with respect to the associated transitions of the voltage waveforms. The average propagation delay is defined as the average of the turn-on delay and the turn-off delay measured from the 1.5 V point of the input to the 1.5 V point of the associated output transition or:

$$t_{pd} = \frac{t_{on} + t_{off}}{2} \text{ ns.}$$

Rise time is defined as the positive going transition of the output from the 1.0 V to the 2.0 V level. Fall time is defined as the negative transition of the output from the 2.0 V to the 1.0 V level.

(2)

$$P_D = \frac{I_{PDL} + I_{PDH}}{2} (V_{CC})$$

where I_{PDL} and I_{PDH} are the typical dc current drains at $V_{CC} = +5.0$ V.

MC400/450 and MC500/550 M TTL* series integrated circuits are electrically interchangeable with SUHL 1† series logic circuits.

SG SF NUMBERS	Description	-55 to +125°C		0 to +75°C	
		Fan-Out = 15	Fan-Out = 7	Fan-Out = 12	Fan-Out = 6
SG40-43	Dual 4-Input NAND Gate	MC500	MC550	MC400	MC450
SG50-53	Expandable 2-Wide 2-2-3-Input AND-OR-INVERT Gate	MC501	MC551	MC401	MC451
SG60-63	Single 8-Input NAND Gate	MC502	MC552	MC402	MC452
SG90-93	2-Wide 3-Input AND-OR-INVERT Gate with Gated Complement	MC503	MC553	MC403	MC453
SG100-103	Expandable 3-Wide 3-Input AND-OR-INVERT Gate	MC504	MC554	MC404	MC454
SG110-113	Expandable 2-Wide 4-Input AND-OR-INVERT Gate	MC505	MC555	MC405	MC455
SG120-123	Expandable 8-Input NAND Gate	MC506	MC556	MC406	MC456
SG130-133	Line Driver	MC507	MC557	MC407	MC457
SG140-143	Quad 2-Input NAND Gate	MC508	MC558	MC408	MC458
SG150-153	4-Wide 3-2-2-3-Input Expander for AND-OR-INVERT Gates	MC509	MC559	MC409	MC459
SG170-173	Dual 4-Input Expander for AND-OR-INVERT Gates	MC510	MC560	MC410	MC460
SG180-183	Dual 4-Input Expander for NAND Gates	MC511	MC561	MC411	MC461
SG190-193	Triple 3-Input NAND Gate	MC512	MC562	MC412	MC462
SF10-13	R-S Flip-Flop	MC513	MC563	MC413	MC463
SF50-53	AND J-K Flip-Flop	MC515	MC565	MC415	MC465
SF60-63	OR J-K Flip-Flop	MC516	MC566	MC416	MC466
SG70-73	Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC520	MC570	MC420	MC470

*Trademark of Motorola Inc.

†Trademark of Sylvania Electric Products, Inc.

MTTL

GENERAL INFORMATION SECTION

DEFINITIONS

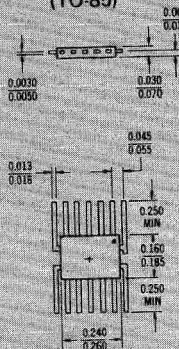
$BV_{in} "0"$	Input breakdown voltage (ON level)
$BV_{in} "1"$	Input breakdown voltage (OFF level)
C_T	Total parasitic capacitance, which includes probe, wiring, and load capacitances
f_{Tog}	Toggle frequency
h_{FE}	Forward beta
I_{B1}, I_{B2}	Base current
I_C	Collector Current
I_F	Input forward current
I_{in}	Input current
I_L	Inverse beta current
I_{max}	Maximum rated power supply current with V_{max} applied
I_O	Output breakdown current
I_{OH}	Output high current
I_{OL}	Output low current
I_{OLK}	Output leakage current
I_{PDH}	Power supply drain with inputs high
I_{PDL}	Power supply drain with inputs low
I_R	Input reverse current with V_R applied
I_{SC}	Short circuit current obtained from device output when one or more inputs are low
P_r	Prime fan-out
PRF	Pulse repetition frequency
PW	Pulse width
R_G	Generator resistance
R_L	Load resistance
Std	Standard fan-out
t_f	Fall time
t_{off}	Turn-off delay time
t_{on}	Turn-on delay time
t_{Post}	The minimal time necessary before the SET, PRESET or RESET inputs can control the flip-flop after the negative clock edge

t_r	Rise time
Δt_{pd}	Average increase in propagation delay per AND gate of expander when connected to an AND-OR-INVERT gate
$\Delta t_{pd}/pF$	Increased propagation delay caused by additional capacitance at expansion points
TP_{in}	Test point at input of device under test
TP_{out}	Test point at output of device under test
V_{amp}	Voltage amplitude
V_{BC}	Base-collector voltage
V_{BE}	Base-emitter voltage
V_C	Collector voltage
V_{CC}	Power supply voltage
V_{CCH}	High power supply voltage
V_{CE}	Collector-emitter voltage
V_{CR}	Collector voltage obtained thru 1.3 k ohm resistor from V_{CC}
V_{CRH}	Collector voltage obtained thru 1.3 k ohm resistor from V_{CCH}
V_{DC}	Voltage obtained with two series diodes tied from collector to ground
V_{E1}, V_{E2}, V_{E3}	Emitter voltage
V_{EN}	Enable voltage level
V_{IH}	Voltage for high input voltage state
V_{IHX}	Reduced supply voltage to hold input above threshold and to prevent noise from entering the device
V_{IL}	Voltage for low input voltage state
V_{INH}	Inhibit voltage level
V_{max}	Maximum rated power supply voltage (V_{CC})
V_O	Offset voltage
V_{OH}	Output high voltage with I_{OH} flowing out of pin
V_{OL}	Output low voltage with I_{OL} flowing into pin
V_{out}	Output voltage
$V_{out} "0"$	Output low voltage with $V_{th} "1"$ applied
$V_{out} "1"$	Output high voltage with $V_{th} "0"$ applied
V_R	Input reverse voltage
$V_{th} "0"$	Logic "0" threshold voltage
$V_{th} "1"$	Logic "1" threshold voltage

PACKAGING

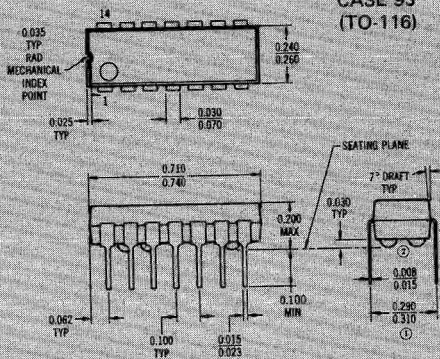
All MTTL integrated circuits are available in the TO-85, 14-lead flat package. MC400 series is also available in the 14-lead dual in-line plastic package. To order the flat package, add suffix "F" to the basic type number; to order plastic package, add suffix "P".

CASE 609
(TO-85)



Lead 1 identified by color dot or by elbow on lead. All leads electrically isolated from package.

CASE 93
(TO-116)

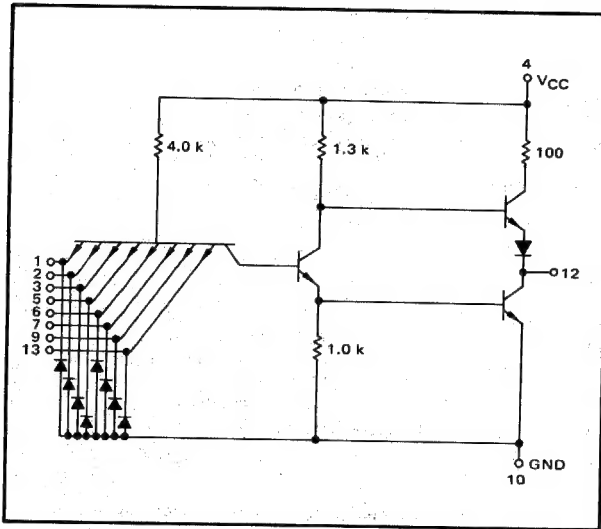


① This dimension is measured at the seating plane.
② 4 Insulating stand-offs are provided.

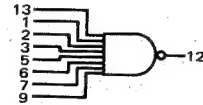
SINGLE 8-INPUT "NAND" GATE

MTTL MC500/400 series

MC502 • MC552
MC402 • MC452



This device is an 8-input NAND gate. It is useful when processing a large number of variables, such as in encoders or decoders.



Positive Logic:

$$12 = 1 \cdot 2 \cdot 3 \cdot 5 \cdot 6 \cdot 7 \cdot 9 \cdot 13$$

Negative Logic:

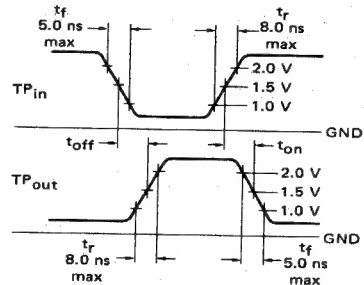
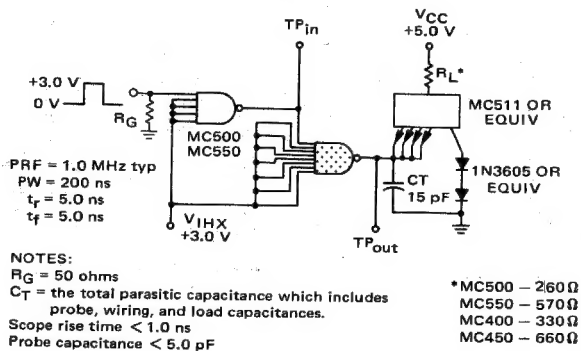
$$12 = 1 + 2 + 3 + 5 + 6 + 7 + 9 + 13$$

Total Power Dissipation = 15 mW typ/pkg
Propagation Delay Time = 12 ns typ

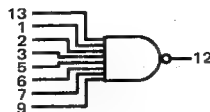
SERIES	INPUT LOADING FACTOR (I_F)	OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
MC502 MC552	1 (-1.33 mA)	15 MC500 series Gates (20 mA) 7 MC500 series Gates (10 mA)	-55°C to +125°C
MC402 MC452	1 (-1.66 mA)	12 MC400 series Gates (20 mA) 6 MC400 series Gates (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUITS

VOLTAGE WAVEFORMS AND DEFINITIONS



Test procedures are shown for only one input of the gate. To complete testing, sequence through remaining inputs in the same manner.



**@ Test
Temperatu**

MC502*, MC552

MC402*, MC452

TEST CONDITIONS														Gnd
mA				Volts										
I _{OL}		I _{OH}		I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}	
Pr*	Std	Pr*	Std											
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-	
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0	
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-	
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-	
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0	
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-	
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:														
I _{OL}	I _{OH}	I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}			
-	-	-	-	-	2,3,5,6, 7,9,13	-	-	-	4	-	-	-	-	1,10
-	-	-	-	-	1	-	-	-	4	-	-	-	-	2,3,5,6,7, 9,10,13
-	-	-	-	-	1	-	-	-	4	-	-	-	-	10
-	-	1	-	-	-	-	-	-	4	-	-	-	-	10
-	-	1	-	-	-	-	-	-	4	-	-	-	-	2,3,5,6,7, 9,10,13
12	-	-	-	-	-	1	-	-	4	-	-	-	-	10
-	12	-	-	-	-	-	1	-	4	-	-	-	-	10
-	-	-	-	-	-	-	-	12	4	-	-	-	-	1,2,3,5,6, 7,9,10,13
-	-	-	-	-	-	-	-	-	4	-	-	-	-	1,2,3,5,6, 7,9,10,13
12	-	-	-	1	-	-	-	-	4	-	-	-	-	10
-	12	-	1	-	-	-	-	-	4	-	-	-	-	10
-	-	-	-	-	-	-	-	-	-	4	-	-	-	1,10
-	-	-	-	-	-	-	-	-	4	-	-	-	-	10
-	-	-	-	-	-	-	-	-	4	-	-	-	-	1,10
Pulse In	Pulse Out													
1	12	-	-	-	-	-	-	-	4	-	-	2,3,5,6, 7,9,13	-	10
1	12	-	-	-	-	-	-	-	4	-	-	2,3,5,6, 7,9,13	-	10
1	12	-	-	-	-	-	-	-	4	-	-	2,3,5,6, 7,9,13	-	10
1	12	-	-	-	-	-	-	-	4	-	-	2,3,5,6, 7,9,13	-	10

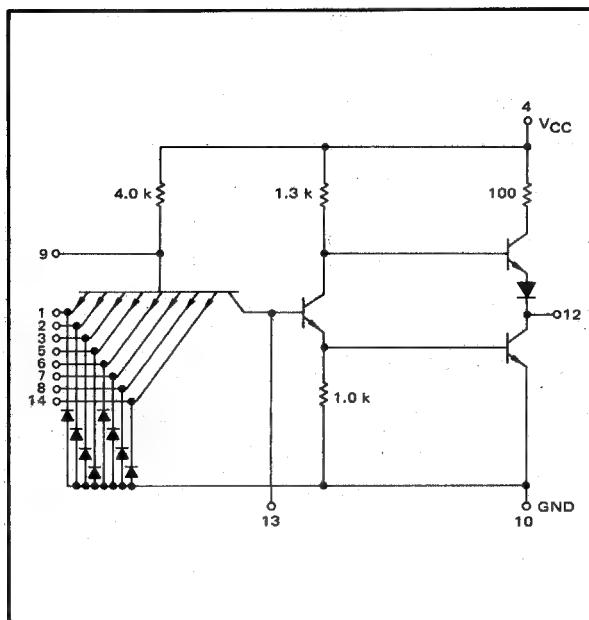
*Prime Fan-Out.

MC502, MC552/MC402, MC452 (continued)

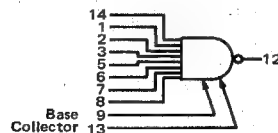
EXPANDABLE 8-INPUT "NAND" GATE

MTTL MC500/400 series

MC506 • MC556
MC406 • MC456



This device consists of an 8-input AND gate driving an output inverter. The base and the collector of the multiple emitter input transistor are available as expander terminals. The number of inputs can be expanded to 20 by using the MC511 series expanders. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

12 = 1 • 2 • 3 • 5 • 6 • 7 • 8 • 14 • Expanders

Negative Logic:

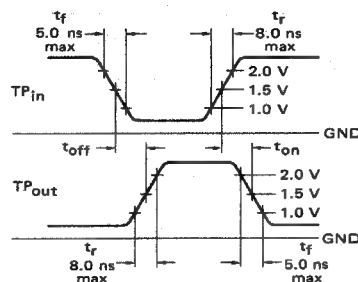
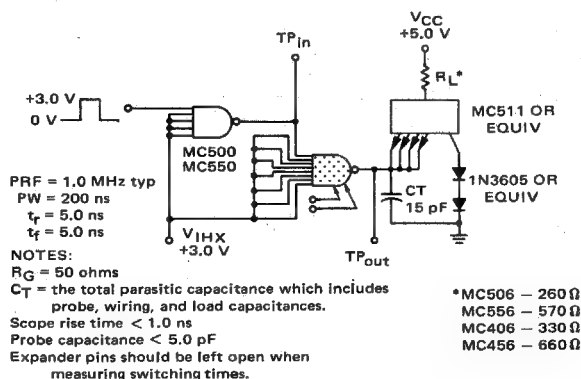
12 = 1 + 2 + 3 + 5 + 6 + 7 + 8 + 14 + Expanders

Total Power Dissipation = 15 mW typ/pkg
Propagation Delay Time = 18 ns typ

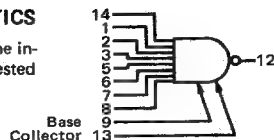
SERIES	INPUT LOADING FACTOR	(I _F)	OUTPUT DRIVE	(I _{OL})	TEMPERATURE RANGE
MC506 MC556	1	(-1.33 mA)	15 MC500 series Gates 7 MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC406 MC456	1	(-1.66 mA)	12 MC400 series Gates 6 MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



Test procedures are shown for only one input of the gate. The other inputs are tested in the same manner.



MC406*, MC456

$$\begin{array}{l} 56 \left\{ \begin{array}{l} -55^\circ \\ +25^\circ \\ +125^\circ \end{array} \right. \\ 56 \left\{ \begin{array}{l} 0^\circ \\ +25^\circ \\ +75^\circ \end{array} \right. \end{array}$$

TEST CONDITIONS														Gnd
mA				Volts										
I _{OL}		I _{OH}		I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}	
Pr*	Std	Pr*	Std											
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-	
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0	
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-	
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-	
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0	
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-	
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:														
I _{OL}	I _{OH}	I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}			
-	-	-	-	-	2,3,5,6, 7,8,14	-	-	-	4	-	-	-	1,10	
-	-	-	-	-	1	-	-	-	4	-	-	-	2,3,5,6,7, 8,10,14	
-	-	-	-	-	1	-	-	-	4	-	-	-	10	
-	-	1	-	-	-	-	-	-	4	-	-	-	10	
-	-	1	-	-	-	-	-	-	4	-	-	-	2,3,5,6,7, 8,10,14	
12	-	-	-	-	-	1	-	-	4	-	-	-	10	
-	12	-	-	-	-	-	1	-	4	-	-	-	10	
-	-	-	-	-	-	-	-	12	4	-	-	-	1,2,3,5,6, 7,8,10,14	
-	-	-	-	-	-	-	-	-	4	-	-	-	1,2,3,5,6, 7,8,10,12,14	
12	-	-	-	1	-	-	-	-	4	-	-	-	10	
-	12	-	1	-	-	-	-	-	4	-	-	-	10	
-	-	-	-	-	-	-	-	-	-	4	-	-	1,10	
-	-	-	-	-	-	-	-	-	4	-	-	-	10	
-	-	-	-	-	-	-	-	-	4	-	-	-	1,10	
Pulse In	Pulse Out													
1	12	-	-	-	-	-	-	-	4	-	-	2,3,5,6, 7,8,14	10	
1	12	-	-	-	-	-	-	-	4	-	-	2,3,5,6, 7,8,14	10	
1	12	-	-	-	-	-	-	-	4	-	-	2,3,5,6, 7,8,14	10	
1	12	-	-	-	-	-	-	-	4	-	-	2,3,5,6, 7,8,14	10	

† Add 3.0 ns for each AND expander (1/2 MC511, MC561, MC411, and MC461) used. Add 2.0 ns for each pF added to either expander points.

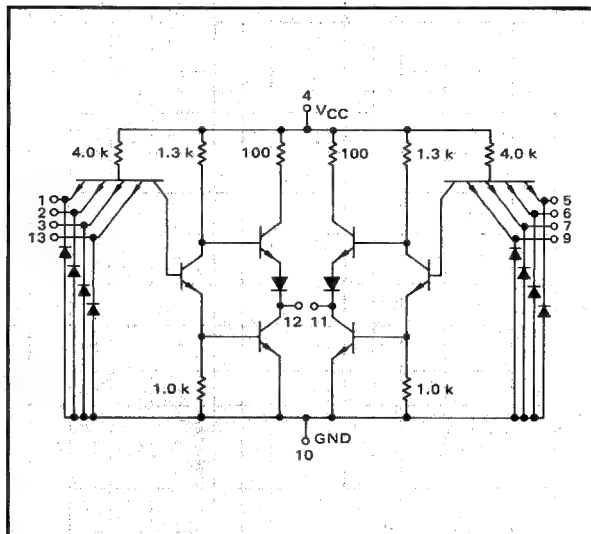
Add 2.0 ns t_{ind} for each pF added to either expander points.

MC506, MC556/MC406, MC456 (continued)

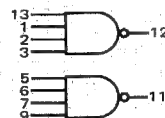
DUAL 4-INPUT "NAND" GATE

MTTL MC500/400 series

MC500 • MC550
MC400 • MC450



This device consists of two 4-input NAND gates. The gates can be cross-coupled to form a multiple-input R-S flip-flop or a circuit for eliminating contact bounce.



Positive Logic:

$$12 = 1 \cdot 2 \cdot 3 \cdot 13$$

Negative Logic:

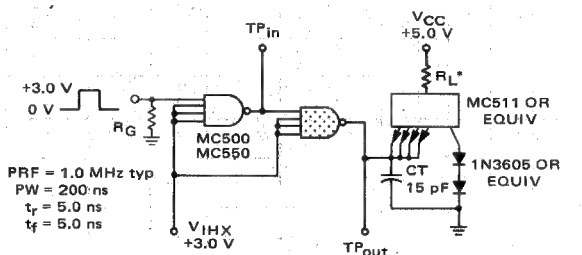
$$12 = 1 + 2 + 3 + 13$$

Total Power Dissipation = 30 mW typ/pkg
Propagation Delay Time = 10 ns typ

SERIES	INPUT LOADING FACTOR	(I _F)	OUTPUT DRIVE	(I _{OL})	TEMPERATURE RANGE
MC500	1	(-1.33 mA)	15 MC500 series Gates	(20 mA)	-55°C to +125°C
MC550			7 MC500 series Gates	(10 mA)	
MC400	1	(-1.66 mA)	12 MC400 series Gates	(20 mA)	0° to +75°C
MC450			6 MC400 series Gates	(10 mA)	

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



NOTES:

R_G = 50 ohms

C_T = the total parasitic capacitance which includes probe, wiring and load capacitances.

Scope rise time < 1.0 ns

Probe capacitance < 5.0 pF

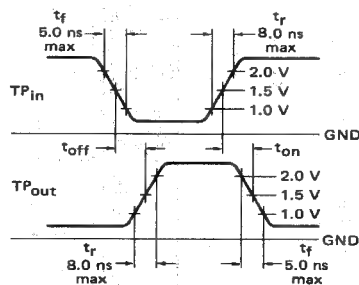
Ground inputs to all gates not under test.

*MC500 - 260 Ω

MC550 - 570 Ω

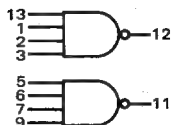
MC400 - 330 Ω

MC450 - 660 Ω



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@ Test Temperature
MC500*, MC550
-55°C
+25°C
+125°C
MC400*, MC450
0°C
+25°C
+75°C

TEST CONDITIONS																		Gnd †
mA						Volts												
I _{OL}		I _{OH}		I _{in}	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th 0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}					
Pr*	Std	Pr*	Std															
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-					
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0					
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-					
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-					
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0					
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-					
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																		Gnd †
I _{OL}		I _{OH}		I _{in}	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th 0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}					
-	-	-	-	-	-	-	2,3,13	-	-	-	4	-	-	1,10				
-	-	-	-	-	-	-	1	-	-	-	4	-	-	2,3,10,13				
-	-	-	-	-	-	-	1	-	-	-	4	-	-	10				
-	-	1	-	-	-	-	-	-	-	-	4	-	-	10				
-	-	1	-	-	-	-	-	-	-	-	4	-	-	2,3,10,13				
12	-	-	-	-	-	-	-	1	-	-	4	-	-	10				
-	12	-	-	-	-	-	-	-	1	-	4	-	-	10				
-	-	-	-	-	-	-	-	-	-	12	4	-	-	1,2,3,10,13				
-	-	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,10,12,13				
12	-	-	-	-	1	-	-	-	-	-	4	-	-	10				
-	12	-	1	-	-	-	-	-	-	-	4	-	-	10				
-	-	-	-	-	-	-	-	-	-	-	-	4	-	1,5,10				
-	-	-	-	-	-	-	-	-	-	-	4	-	-	10†				
-	-	-	-	-	-	-	-	-	-	-	4	-	-	1,5,10				
Pulse In		Pulse Out																10
1	12	-	-	-	-	-	-	-	-	-	4	-	2,3,13					
1	12	-	-	-	-	-	-	-	-	-	4	-	2,3,13					
1	12	-	-	-	-	-	-	-	-	-	4	-	2,3,13					
1	12	-	-	-	-	-	-	-	-	-	4	-	2,3,13	10				

* Prime Fan-Out.

† Ground inputs to gates not under test during ALL tests, unless otherwise noted.

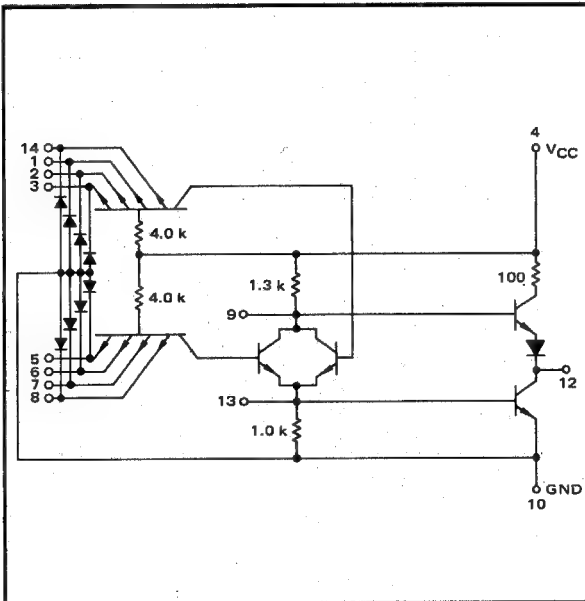
‡ The inputs of all gates must be ungrounded.

MC500, MC550/MC400, MC450 (continued)

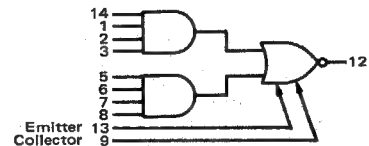
**EXPANDABLE 2-WIDE 4-INPUT
"AND-OR-INVERT" GATE**

MTTL MC500/400 series

**MC505 • MC555
MC405 • MC455**



This device consists of two 4-input AND gates ORed together and driving an output inverter. The ORing nodes are available for expansion and up to 10 AND gates can be ORed together using the MC509 or MC510 series expanders. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

$$12 = (1 \cdot 2 \cdot 3 \cdot 14) + (5 \cdot 6 \cdot 7 \cdot 8) + (\text{Expanders})$$

Negative Logic:

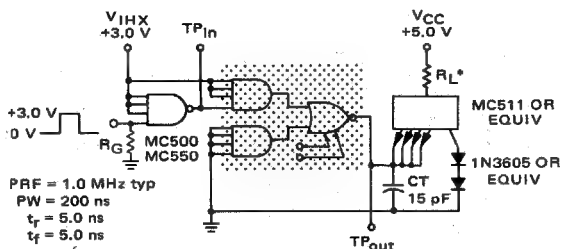
$$12 = (1 + 2 + 3 + 14) \cdot (5 + 6 + 7 + 8) \cdot (\text{Expanders})$$

Total Power Dissipation = 20 mW typ/pkg
Propagation Delay Time = 12 ns typ

SERIES	INPUT LOADING FACTOR (I _F)	OUTPUT DRIVE (I _{OL})	TEMPERATURE RANGE
MC505 MC555	1 (-1.33 mA)	15 MC500 series Gates (20 mA) 7 MC500 series Gates (10 mA)	-55°C to +125°C
MC400 MC450	1 (-1.66 mA)	12 MC400 series Gates (20 mA) 6 MC400 series Gates (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



NOTES:

R_G = 50 ohms

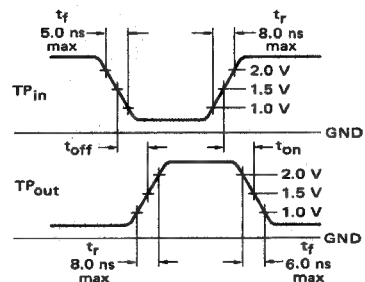
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.

Scope rise time < 1.0 ns

Probe capacitance < 5.0 pF

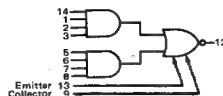
Expander pins should be left open when measuring switching times.

* MC505 - 260 Ω
MC555 - 570 Ω
MC405 - 330 Ω
MC455 - 660 Ω



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the device. To complete testing sequence through remaining inputs in the same manner.



		@ Test Temperature	
MC505*, MC555	-55°C	Pr*	Std
	+25°C	Pr*	Std
	+125°C	Pr*	Std
MC405*, MC455	0°C	Pr*	Std
	+25°C	Pr*	Std
	+75°C	Pr*	Std

TEST CONDITIONS																	
mA						Volts											
I _{OL}		I _{OH}		I _{in}		V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}			
Pr*	Std	Pr*	Std	Pr*	Std												
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-	-	-	-	-
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0	-	-	-	-
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-	-	-	-	-
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-	-	-	-	-
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0	-	-	-	-
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-	-	-	-	-

Characteristic	Symbol	Pin Under Test	MC505, MC555 Test Limits						MC405, MC455 Test Limits						Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:														Gnd																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																					
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C			I _{OL}	I _{OH}	I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																								
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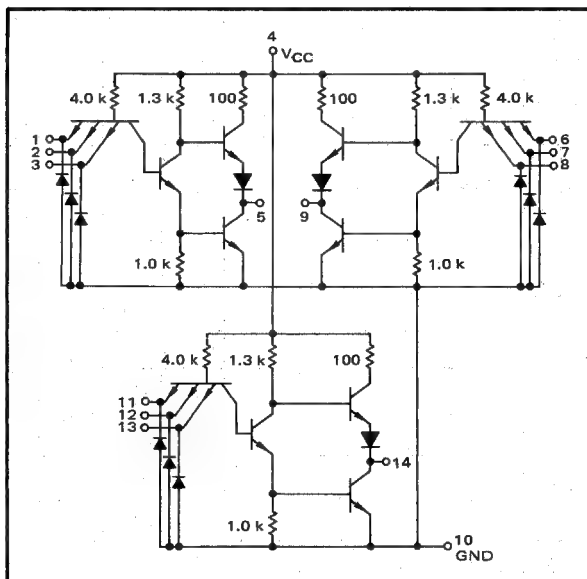
* Prime Fan-Out

MC505, MC555/MC405, MC455 (continued)

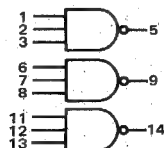
TRIPLE 3-INPUT "NAND" GATE

MTTL MC500/400 series

MC512 • MC562
MC412 • MC462



This device consists of a 3-input AND gate driving an output inverter. This gate can be used to build a pulse shaping network for interfacing with discrete component circuits.



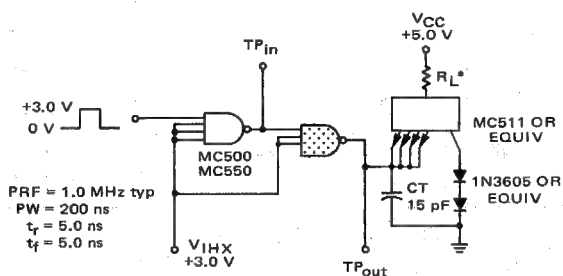
Positive Logic: $5 = 1 \cdot 2 \cdot 3$
Negative Logic: $5 = \overline{1} + \overline{2} + \overline{3}$

Total Power Dissipation = 45 mW typ/pkg
Propagation Delay Time = 10 ns typ

SERIES	INPUT LOADING FACTOR (I _F)	OUTPUT DRIVE (I _{OL})	TEMPERATURE RANGE
MC512 MC562	1 (-1.33 mA)	15 MC500 series Gates (20 mA) 7 MC500 series Gates (10 mA)	-55°C to +125°C
MC412 MC462	1 (-1.66 mA)	12 MC400 series Gates (20 mA) 6 MC400 series Gates (10 mA)	0°C to +75°C

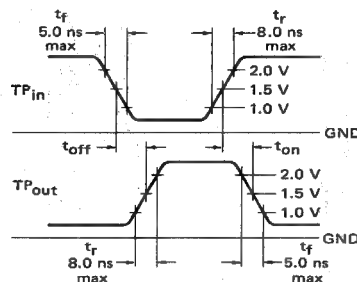
SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



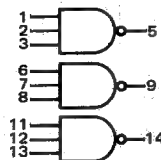
NOTES:
RG = 50 ohms
CT = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
Ground inputs to all gates not under test.

*MC512 - 260Ω
MC562 - 570Ω
MC412 - 330Ω
MC462 - 660Ω



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@ Test
Temperature

MC512*, MC562
 {
 -55°C
 +25°C
 +125°C
 MC412*, MC462
 {
 0°C
 +25°C
 +75°C

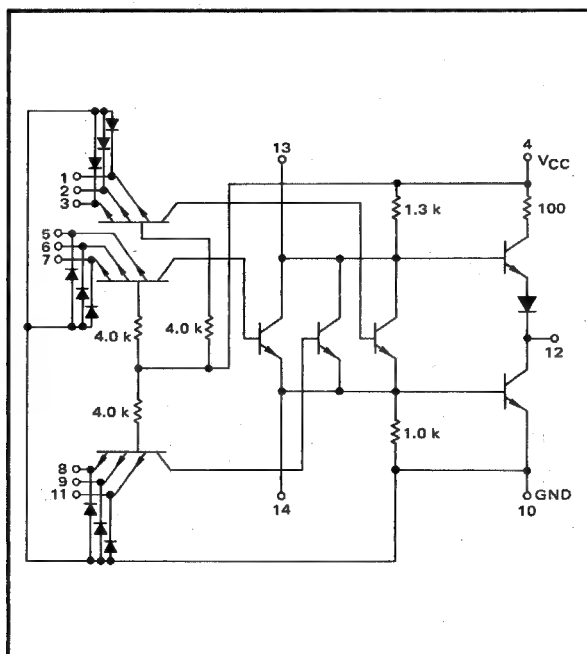
Characteristic		Symbol	Pin Under Test	TEST CONDITIONS												TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:										Unit	Gnd †	
				mA						Volts																		
				I _{OL}		I _{OH}		I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}											
				Pr*	Std	Pr*	Std																					
Input																												
Forward Current	I _F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	-	-	-	-	-	-	1,10	
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	-	-	-	-	2,3,10	
Inverse Beta Current	I _L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	-	-	-	-	10	
Breakdown Voltage	BV _{in "0"}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	-	-	-	-	-	-	-	-	-	10	
	BV _{in "1"}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	-	-	-	-	-	-	-	-	-	2,3,10	
Output																												
Output Voltage	V _{out "0"}	5	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	5	-	-	-	-	-	-	-	-	-	-	10	
	V _{out "1"}	5	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	5	-	-	-	-	-	-	-	-	-	10	
Leakage Current	I _{OLK}	5	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	-	-	-	1,2,3,10	
Short-Circuit Current	I _{SC}	5	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	-	-	1,2,3,5,10	
Output Voltage	V _{OL}	5	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	5	-	-	-	-	-	-	-	-	-	-	10	
	V _{OH}	5	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	5	-	-	-	-	-	-	-	-	-	10	
Power Requirements																												
(Total Device)																												
Maximum Power Supply Current	I _{max}	4	-	-	-	15	-	-	-	-	-	-	15	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	1,6,10,11	
Power Supply Drain	I _{PDH}	4	-	18	-	18	-	18	-	22.5	-	22.5	-	22.5	mAdc	-	-	-	-	-	-	-	-	-	-	-	10 ‡	
	I _{PDL}	4	-	9.0	-	9.0	-	9.0	-	9.0	-	9.0	-	9.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	1,6,10,11	
Switching Parameters																												
Turn-On Delay	t _{on}	1,5	-	-	-	20	-	-	-	-	-	-	20	-	-	ns	Pulse In	Pulse Out										
Turn-Off Delay	t _{off}	1,5	-	-	-	20	-	-	-	-	-	-	20	-	-	ns	1	5	-	-	-	-	-	-	-	-	10	
Rise Time	t _r	1,5	-	-	-	8.0	-	-	-	-	-	-	8.0	-	-	ns	1	5	-	-	-	-	-	-	-	-	10	
Fall Time	t _f	1,5	-	-	-	5.0	-	-	-	-	-	-	5.0	-	-	ns	1	5	-	-	-	-	-	-	-	-	10	

* Prime Fan-Out † Ground inputs to gates not under test, during ALL tests unless otherwise noted. ‡ The inputs to all gates must be ungrounded.

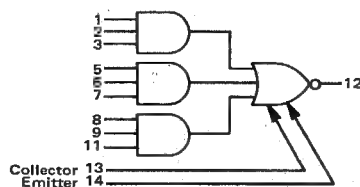
EXPANDABLE 3-WIDE 3-INPUT "AND-OR-INVERT" GATE

MTTL MC500/400 series

MC504 • MC554
MC404 • MC454



This device consists of three 3-input AND gates ORed together driving an output inverter. The common ORing nodes are available for expansion, and up to 10 AND gates can be ORed together using the MC509 or the MC510 series expanders. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

$$12 = (1 \cdot 2 \cdot 3) + (5 \cdot 6 \cdot 7) + (8 \cdot 9 \cdot 11) + (\text{Expanders})$$

Negative Logic:

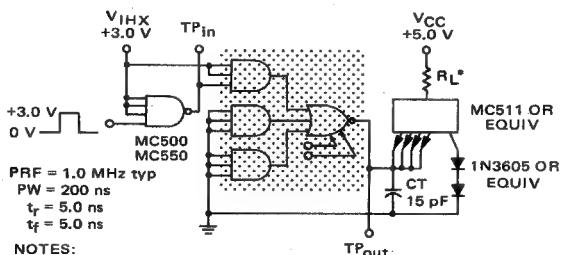
$$12 = (1 + 2 + 3) \cdot (5 + 6 + 7) \cdot (8 + 9 + 11) \cdot (\text{Expanders})$$

Total Power Dissipation = 25 mW typ/pkg
Propagation Delay Time = 12 ns typ

SERIES	INPUT LOADING FACTOR (I_F)	OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
MC504 MC554	1 (-1.33 mA)	15 MC500 series Gates 7 MC500 series Gates (20 mA) (10 mA)	-55°C to +125°C
MC404 MC454	1 (-1.66 mA)	12 MC400 series Gates 6 MC400 series Gates (20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



PRF = 1.0 MHz typ
PW = 200 ns
 t_r = 5.0 ns
 t_f = 5.0 ns

NOTES:

R_G = 50 ohms

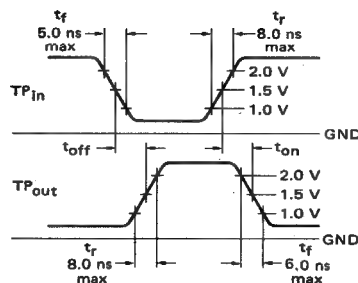
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.

Scope rise time < 1.0 ns

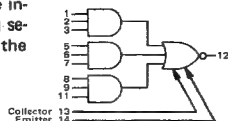
Probe capacitance < 5.0 pF

Expander pins should be left open when measuring switching times.

* MC504 - 260 Ω
MC554 - 570 Ω
MC404 - 330 Ω
MC454 - 660 Ω



Test procedures are shown for only one input of the device. To complete testing sequence through remaining inputs in the same manner.



MC404*, MC454

@ Test Temperature

TEST CONDITIONS													
mA				Volts									
I_{OL}		I_{OH}		I_{in}	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{CC}	V_{CCH}	V_{IHx}
Pr*	Std	Pr*	Std										
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-

Characteristic	Symbol	Pin Under Test	MC504, MC554 Test Limits						MC404, MC454 Test Limits						Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																															
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C			I _{OL}	I _{OH}	I _{in}	V _{IL}	V _{IH}	V _R	V _{In1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}	Gnd																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
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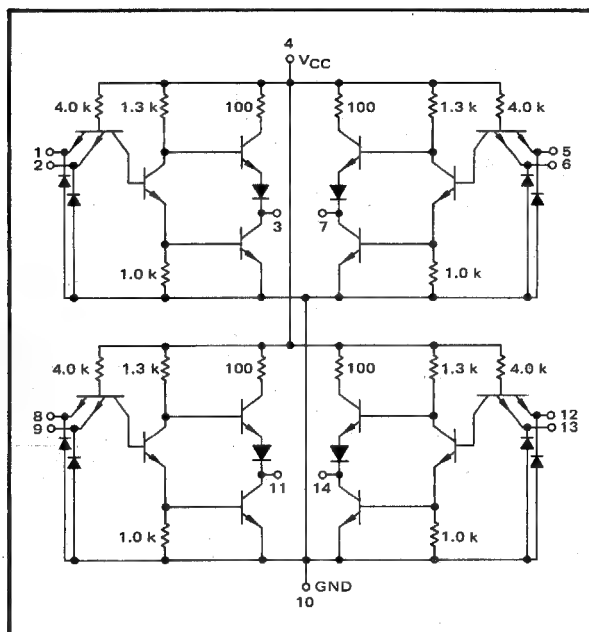
* Prime Fan-Out

MC504, MC554/MC404, MC454 (continued)

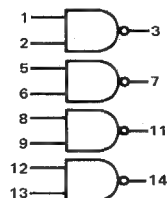
QUAD 2-INPUT "NAND" GATE

MTTL MC500/400 series

MC508 • MC558
MC408 • MC458



This device consists of four 2-input NAND gates. The four gates in a single package represent increased functional flexibility. For example, a dual set-reset flip-flop may be obtained if each pair of gates is externally cross-coupled.



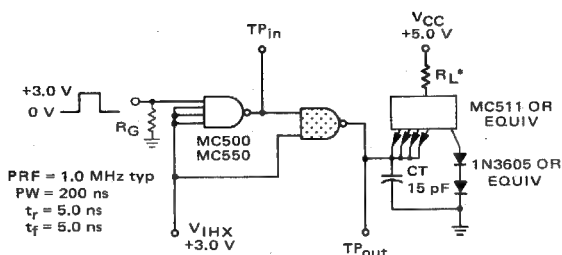
Positive Logic: $3 = \overline{1 \cdot 2}$
 Negative Logic: $3 = \overline{1} + \overline{2}$

Total Power Dissipation = 60 mW typ/pkg
 Propagation Delay Time = 10 ns typ

SERIES	INPUT LOADING FACTOR (I_F)	OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
MC508 MC558	1 (-1.33 mA)	15 MC500 series Gates 7 MC500 series Gates (20 mA) (10 mA)	-55°C to +125°C
MC408 MC458	1 (-1.66 mA)	12 MC400 series Gates 6 MC400 series Gates (20 mA) (10 mA)	0° to +75°C

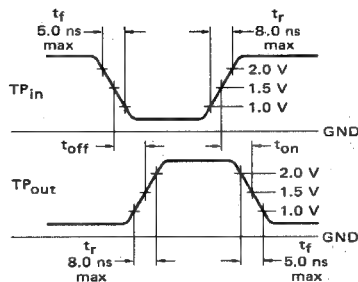
SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



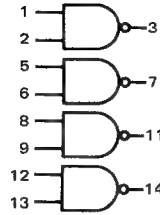
NOTES:
 $R_G = 50$ ohms
 C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
 Scope rise time < 1.0 ns
 Probe capacitance < 5.0 pF
 Ground inputs to all gates not under test.

*MC508 - 260 Ω
 MC558 - 570 Ω
 MC408 - 330 Ω
 MC458 - 660 Ω



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in a similar manner. Further, test procedures are shown for only one input of the gate being tested. The other input is tested in the same manner.



@ Test Temperature
MC508*, MC558
MC408*, MC458

		TEST CONDITIONS																		
		mA						Volts												
		I_{OL}		I_{OH}		I_{in}	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{CC}	V_{CCH}	V_{IHx}					
		Pr*	Std	Pr*	Std															
		-55°C																		
		20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-	-				
		20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0	-				
		+25°C																		
		20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-	-				
		20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-	-				
		0°C																		
		20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0	-				
		20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-	-				
		+75°C																		
		20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-	-				
		TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																		
		I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{CC}	V_{CCH}	V_{IHx}	Gnd†						
Characteristic	Symbol	Pin Under Test	MCS08, MCS58 Test Limits						MC408, MC458 Test Limits						Unit					
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C							
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max						
Input																				
Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	1,10	
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μ Adc	-	-	-	2,10	
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μ Adc	-	-	-	10	
Breakdown Voltage	$BV_{in"0"}$	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	10	
	$BV_{in"1"}$	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	2,10	
Output																				
Output Voltage	$V_{out"0"}$	3	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	3	-	-	10	
	$V_{out"1"}$	3	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	3	-	10	
Leakage Current	I_{OLK}	3	-	250	-	250	-	250	-	250	-	250	-	250	μ Adc	-	-	-	1,2,10	
Short-Circuit Current	I_{SC}	3	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	1,2,3,10	
Output Voltage	V_{OL}	3	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	3	-	-	10	
	V_{OH}	3	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	3	-	10	
Power Requirements																				
(Total Device)																				
Maximum Power Supply Current	I_{max}	4	-	-	-	20	-	-	-	-	20	-	-	-	mAdc	-	-	-	1,5,8,10,12	
Power Supply Drain	I_{PDH}	4	-	24	-	24	-	24	-	30	-	30	-	30	mAdc	-	-	-	10†	
	I_{PDL}	4	-	12	-	12	-	12	-	12	-	12	-	12	mAdc	-	-	-	1,5,8,10,12	
Switching Parameters																				
Turn-On Delay	t_{on}	1,3	-	-	-	20	-	-	-	-	20	-	-	-	ns	Pulse In	Pulse Out	-	10	
Turn-Off Delay	t_{off}	1,3	-	-	-	20	-	-	-	-	20	-	-	-	ns	1	3	-	10	
Rise Time	t_r	1,3	-	-	-	8.0	-	-	-	-	8.0	-	-	-	ns	1	3	-	10	
Fall Time	t_f	1,3	-	-	-	5.0	-	-	-	-	5.0	-	-	-	ns	1	3	-	10	

* Prime Fan-Out.

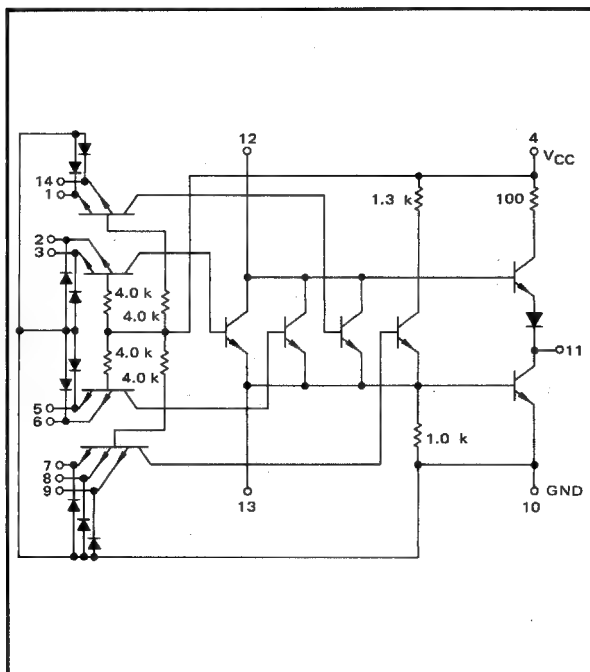
† Ground inputs to gates not under test, during ALL tests unless otherwise noted.

‡ The inputs to all gates must be ungrounded.

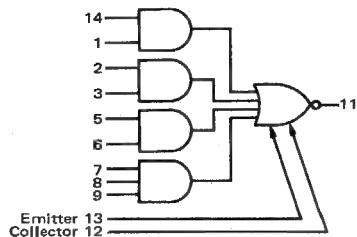
**EXPANDABLE 4-WIDE
2-2-2-3 INPUT
"AND-OR-INVERT" GATE**

MTTL MC500/400 series

**MC501 • MC551
MC401 • MC451**



This device consists of three 2-input and one 3-input AND gates internally ORed together and then inverted to provide the output. The common ORing nodes are available for expansion and up to 10 AND gates can be ORed together using the MC509 and the MC510 series expanders. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

$$11 = (14 \cdot 1) + (2 \cdot 3) + (5 \cdot 6) + (7 \cdot 8 \cdot 9) + (\text{Expanders})$$

Negative Logic:

$$11 = (14 + 1) \cdot (2 + 3) \cdot (5 + 6) \cdot (7 + 8 + 9) \cdot (\text{Expanders})$$

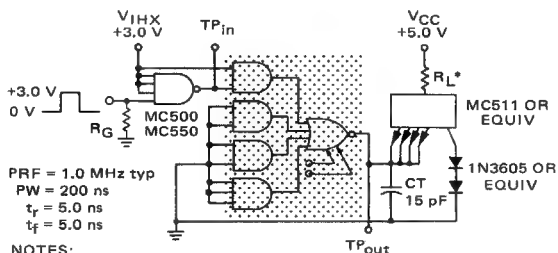
Total Power Dissipation = 30 mW typ/pkg

Propagation Delay Time = 12 ns typ

SERIES	INPUT LOADING FACTOR	(I _I)	OUTPUT DRIVE	(I _{OL})	TEMPERATURE RANGE
MC501 MC551	1	(-1.33 mA)	15 MC500 series Gates 7 MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC401 MC451	1	(-1.66 mA)	12 MC400 series Gates 6 MC400 series Gates	(20 mA) (10 mA)	0°C to +75°C

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



PRF = 1.0 MHz typ

PW = 200 ns

$t_r = 5.0$ ns

$t_f = 5.0$ ns

NOTES:

$R_G = 50$ ohms

C_T = the total parasitic capacitance which includes probe, wiring and load capacitances.

Scope rise time < 1.0 ns

Probe capacitance < 5.0 pF

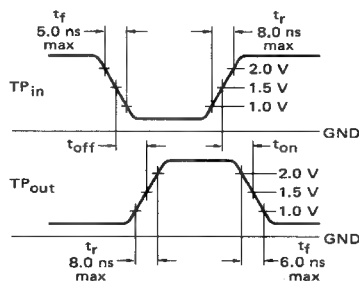
Expander pins should be left open when measuring switching times.

*MC501 - 260 Ω

MC551 - 570 Ω

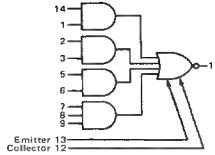
MC401 - 330 Ω

MC451 - 660 Ω



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one input of the device. To complete testing, sequence through remaining inputs in a similar manner.



@ Test Temperature
 MC501*, MC551
 -55°C
 +25°C
 +125°C
 MC401*, MC451
 0°C
 +25°C
 +75°C

TEST CONDITIONS																
mA									Volts							
I _{OL}		I _{OH}		I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}			
Pr*	Std	Pr*	Std													
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-			
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0			
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-			
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-			
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0			
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-			
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																
	I _{OL}	I _{OH}	I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}	Gnd			
c	-	-	-	-	-	14	-	-	-	4	-	-	1,2,3,5,6,7,8,9,10			
c	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7,8,9,10,14			
c	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7,8,9,10			
t	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7,8,9,10			
t	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7,8,9,10,14			
t	11	-	-	-	-	-	1	-	-	4	-	-	2,3,5,6,7,8,9,10			
t	-	11	-	-	-	-	-	1	-	4	-	-	2,3,5,6,7,8,9,10			
c	-	-	-	-	-	-	-	-	-	11	4	-	-	1,2,3,5,6,7,8,9,10,14		
c	-	-	-	-	-	-	-	-	-	4	-	-	-	1,2,3,5,6,7,8,9,10,11,14		
t	11	-	-	-	1	-	-	-	-	4	-	-	2,3,5,6,7,8,9,10			
t	-	11	-	1	-	-	-	-	-	4	-	-	2,3,5,6,7,8,9,10			
c	-	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6,7,8,9,10,14		
c	-	-	-	-	-	-	-	-	-	4	-	-	-	10		
c	-	-	-	-	-	-	-	-	-	4	-	-	-	1,2,3,5,6,7,8,9,10,14		
	Pulse In	Pulse Out														
	1	11								4	-	-	14	2,3,5,6,7,8,9,10		
	1	11								4	-	-	14	2,3,5,6,7,8,9,10		
	1	11								4	-	-	14	2,3,5,6,7,8,9,10		
	1	11								4	-	-	14	2,3,5,6,7,8,9,10		

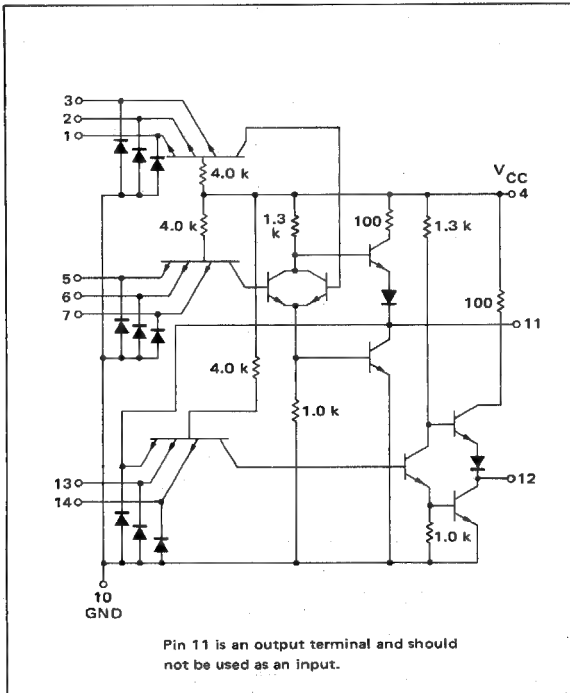
* Prime Fan-Out.

MC501, MC551/MC401, MC451 (continued)

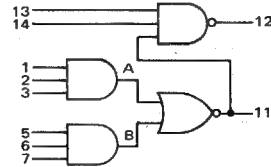
**2-WIDE 3-INPUT
"AND-OR-INVERT" GATE
WITH GATED COMPLEMENT**

MTTL MC500/400 series

**MC503 • MC553
MC403 • MC453**



This device is the only gate of the basic positive AND-OR-INVERT series that includes an additional 3-input AND-INVERT function on the output. This configuration provides the output and a gated complement in a single package. This device is useful in the design of adders, subtractors and one-shot multi-vibrators.



Positive Logic

$$11 = \overline{(1 \cdot 2 \cdot 3)} + \overline{(5 \cdot 6 \cdot 7)}$$

$$12 = \overline{11 \cdot 13 \cdot 14}$$

$$12 = (1 \cdot 2 \cdot 3) + (5 \cdot 6 \cdot 7) + \overline{13} + \overline{14}$$

Total Power Dissipation = 35 mW typ/pkg

Propagation Delay Times = 11 ns typ (Pin 1 to Pin 11)

10 ns typ (Pin 11 to Pin 12)

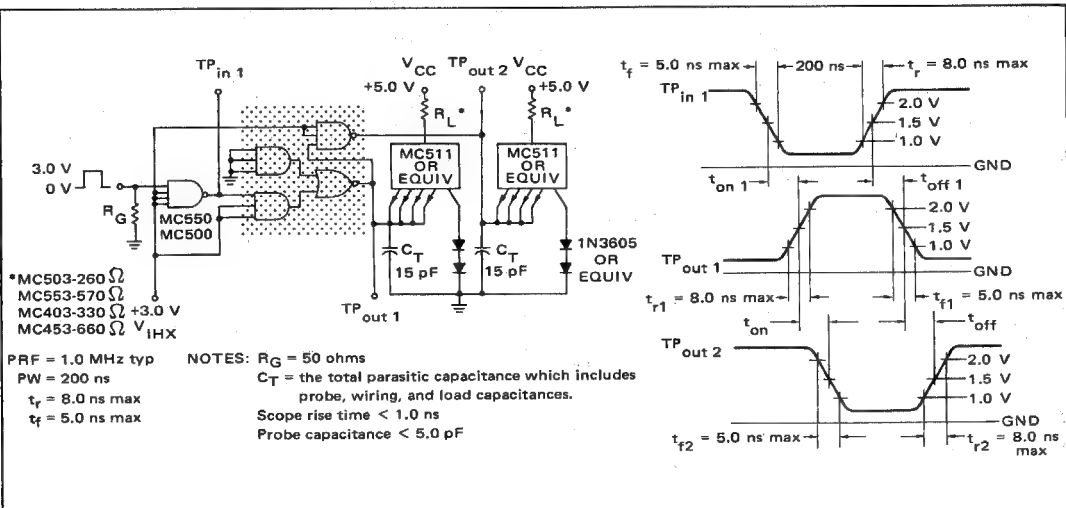
TRUTH TABLE

A	B	OUTPUT PIN # 11	PIN # 13	PIN # 14	OUTPUT PIN # 12
0	1	0	0	0	1
1	0	0	0	1	1
0	1	0	1	0	1
1	0	0	1	1	1
0	0	1	0	0	1
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	0

SERIES	INPUT LOADING FACTOR (I _F)	OUTPUT DRIVE (I _{OL})	TEMPERATURE RANGE
MC503 MC553	1 (-1.33 mA)	15 MC500 Series Gates (20 mA) 7 MC500 Series Gates (10 mA)	-55°C to +125°C
MC403 MC453	1 (-1.66 mA)	12 MC400 Series Gates (20 mA) ■ MC400 Series Gates (10 mA)	0°C to +75°C

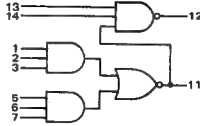
SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the AND-OR-INVERT gate, plus one input of the gated complement. To complete testing, sequence through remaining inputs in the same manner.



@ Test Temperature

MC503*, MC553

MC403*, MC453

		TEST CONDITIONS															Gnd
		mA				Volts											
		I _{OL}		I _{OH}		I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}		
Pr*	Std	Pr*	Std														
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	8.0	-				
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0				
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	8.0	-				
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	7.0	-				
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0				
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	7.0	-				
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																	
I _{OL}		I _{OH}		I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}				
-	-	-	-	-	-	-	2,3	-	-	-	4	-	-	1,5,6,7,10			
-	-	-	-	-	-	-	13	-	-	-	4	-	-	1,2,3,5,6,7,10			
-	-	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7,10			
-	-	-	-	-	-	-	14	-	-	-	4	-	-	10,13			
-	-	-	-	-	-	-	1	-	-	-	4	-	-	5,6,7,10			
-	-	-	-	-	-	-	14	-	-	-	4	-	-	1,2,3,5,6,7,10			
-	-	-	-	1	-	-	-	-	-	-	4	-	-	5,6,7,10			
-	-	-	-	14	-	-	-	-	-	-	4	-	-	1,2,3,5,6,7,10			
-	-	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7,10			
-	-	-	-	14	-	-	-	-	-	-	4	-	-	10,13			
11	-	-	-	-	-	-	-	1	-	-	4	-	-	5,6,7,10			
12	-	-	-	-	-	-	-	14	-	-	4	-	-	1,2,3,5,6,7,10			
-	11	-	-	-	-	-	-	-	1	-	4	-	-	5,6,7,10			
-	12	-	-	-	-	-	-	-	14	-	4	-	-	1,2,3,5,6,7,10			
-	-	-	-	-	-	-	-	-	-	11	4	-	-	1,2,3,5,6,7,10			
-	-	-	-	-	-	-	-	-	-	12	4	-	-	10,13,14			
-	-	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6,7,10,11			
-	-	-	-	-	-	-	-	-	-	-	4	-	-	10,12,13,14			
-	11	-	1	-	-	-	-	-	-	-	4	-	-	5,6,7,10			
-	12	-	14	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6,7,10			
11	-	-	-	-	1	-	-	-	-	-	4	-	-	5,6,7,10			
12	-	-	-	-	14	-	-	-	-	-	4	-	-	1,2,3,5,6,7,10			

MC503, MC553/MC403, MC453 (continued)

ELECTRICAL CHARACTERISTICS (continued)

@ Test
Temperature

MC503*, MC553 {
 -55°C
 +25°C
 +125°C
 MC403*, MC453 {
 0°C
 +25°C
 +75°C

TEST CONDITIONS														Gnd
mA					Volts									
I _{OL}		I _{OH}		I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}	
Pr*	Std	Pr*	Std											
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	8.0	-	
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0	
20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	8.0	-	
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	7.0	-	
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0	
20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	7.0	-	
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:														Gnd
I _{OL}	I _{OH}	I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}			
-	-	-	-	-	-	-	-	-	-	4	-	1, 2, 3, 5, 6, 7, 10, 13, 14		
-	-	-	-	-	-	-	-	-	-	4	-	10		
-	-	-	-	-	-	-	-	-	-	4	-	1, 2, 3, 5, 6, 7, 10		
-	-	-	-	-	-	-	-	-	-	4	-	1, 2, 3, 5, 6, 7, 10, 13, 14		
Pulse In	Pulse Out	-	-	-	-	-	-	-	-	4	-	2, 3, 13, 14	5, 6, 7, 10	
1	11	-	-	-	-	-	-	-	-	4	-	2, 3, 13, 14	5, 6, 7, 10	
1	12	-	-	-	-	-	-	-	-	4	-	2, 3, 13, 14	5, 6, 7, 10	
1	11	-	-	-	-	-	-	-	-	4	-	2, 3, 13, 14	5, 6, 7, 10	
1	12	-	-	-	-	-	-	-	-	4	-	2, 3, 13, 14	5, 6, 7, 10	
1	11	-	-	-	-	-	-	-	-	4	-	2, 3, 13, 14	5, 6, 7, 10	
1	12	-	-	-	-	-	-	-	-	4	-	2, 3, 13, 14	5, 6, 7, 10	
1	11	-	-	-	-	-	-	-	-	4	-	2, 3, 13, 14	5, 6, 7, 10	
1	12	-	-	-	-	-	-	-	-	4	-	2, 3, 13, 14	5, 6, 7, 10	

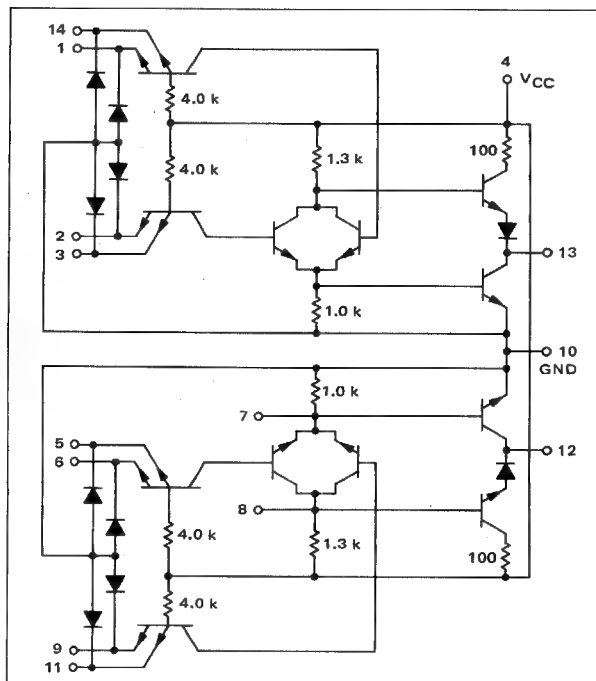
Characteristic	Symbol	Pin Under Test	MC503, MC553 Test Limits						MC403, MC453 Test Limits						Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:													Gnd																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																														
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C			I _{OL}	I _{OH}	I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																
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Power Requirements (Total Device)																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																											

* Prime Fan-Out

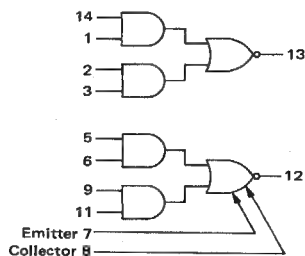
EXPANDABLE DUAL 2-WIDE 2-INPUT "AND-OR-INVERT" GATE

MTTL MC500/400 series

MC520 • MC570
MC420 • MC470



One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together and driving an output inverter with the ORing nodes made available for expansion. Up to 10 AND gates can be ORed together using the MC509 or MC510 expander series. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

$$13 = (1 \cdot 14) + (2 \cdot 3)$$

$$12 = (5 \cdot 6) + (9 \cdot 11) + (\text{Expander})$$

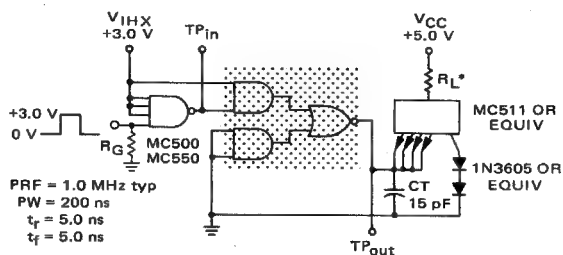
Total Power Dissipation = 40 mW typ/pkg

Propagation Delay Time = 12 ns typ

SERIES	INPUT LOADING FACTOR	(I _F)	OUTPUT DRIVE	(I _{OL})	TEMPERATURE RANGE
MC520 MC570	1	(-1.33 mA)	15 MC500 series Gates 7 MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC420 MC470	1	(-1.66 mA)	12 MC400 series Gates 6 MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



PRF = 1.0 MHz typ
PW = 200 ns
t_r = 5.0 ns
t_f = 5.0 ns

NOTES:

R_G = 50 ohms

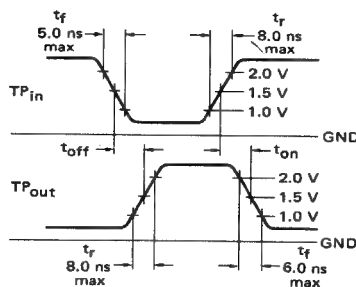
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.

Scope rise time < 1.0 ns

Probe capacitance < 5.0 pF

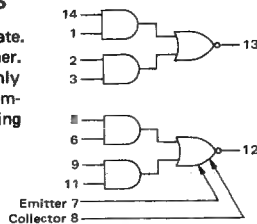
When checking expander side, expander pins should be open.

*MC520 - 260 Ω
MC570 - 570 Ω
MC420 - 330 Ω
MC470 - 660 Ω



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@ Test Temperature

MC520*, MC570
-55°C
+25°C
+125°C
MC420*, MC470
0°C
+25°C
+75°C

Characteristic	Symbol	Pin Under Test	MC520, MC570 Test Limits						MC420, MC470 Test Limits						Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:													Gnd†																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
			-55°C						+25°C							+75°C						I _{OL}	I _{OH}	I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}		V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																														
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* Prime Fan-Out

† Ground inputs to gates not under test during ALL tests unless otherwise noted.

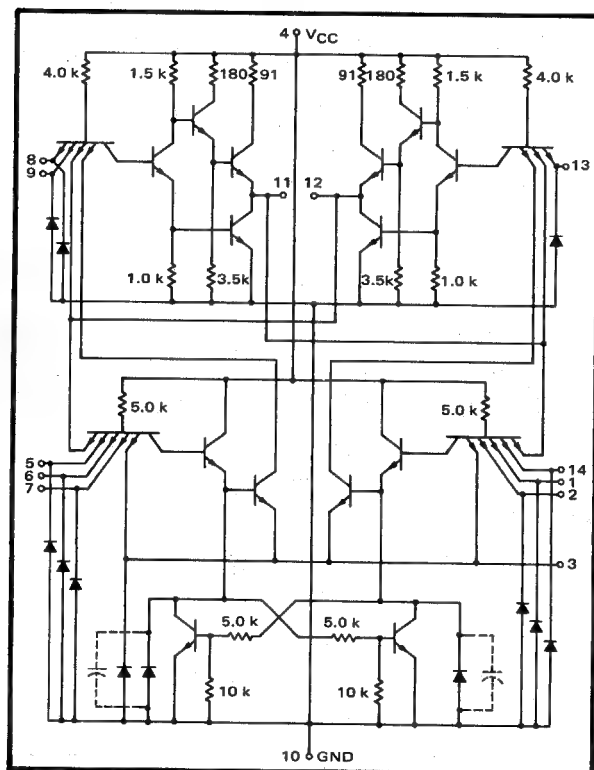
‡ The inputs to all gates must be ungrounded.

MC520, MC570/MC420, MC470 (continued)

"AND" J-K FLIP-FLOP

MTTL MC500/400 series

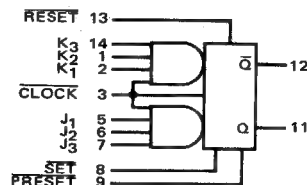
MC515 • MC565
MC415 • MC465



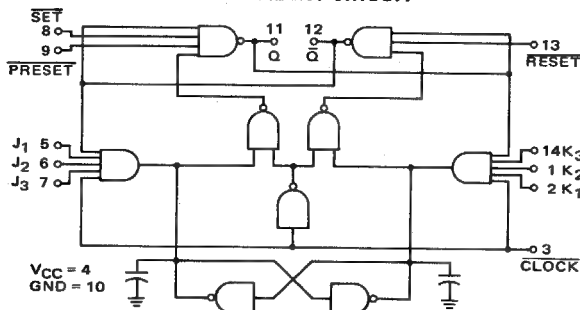
The MC415, MC465, MC515, and MC565 are clocked flip-flops that trigger on the negative edge and perform the J-K logic function. Each flip-flop has an AND input gating configuration consisting of three J inputs ANDed together and three K inputs ANDed together. The multiple J and K inputs minimize the requirements for external gating in counters and certain other applications. A direct SET, PRESET, and RESET are also available.

In normal operation, information is changed on the J and K inputs while the clock is in the low state, since the inputs are inhibited in this condition. Information is read into a temporary memory when the clock is in the high state. When the clock goes low, the information is transferred to the bistable section and the Q and \bar{Q} outputs respond accordingly. The information on the J and K inputs should not be changed while the clock is in the high state. Each flip-flop can be set or reset directly by applying the low state to the direct SET, PRESET, or RESET inputs.

Since each flip-flop is a charge-storage device, there is a restriction on the clock fall time that must be observed.



EQUIVALENT CIRCUIT



J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$$\text{Where } J = J_1 \cdot J_2 \cdot J_3 \\ K = K_1 \cdot K_2 \cdot K_3$$

Total Power Dissipation \pm 40 mW typ/pkg

Switching Times:

$t_{on} = 25$ ns typ

$t_{off} = 13$ ns typ

SERIES	INPUT LOADING FACTOR (I _F)				OUTPUT DRIVE (I _{OL})	TEMPERATURE RANGE
	CLOCK	ALL OTHER	CLOCK	ALL OTHER		
MC515 MC565	1.5	1	(-2.0 mA)	(-1.33 mA)	15 MC500 series Gates (20 mA) 7 MC500 series Gates (10 mA)	-55°C to +125°C
MC415 MC465	1.5	1	(-2.5 mA)	(-1.66 mA)	12 MC400 series Gates (20 mA) 6 MC400 series Gates (10 mA)	0°C to +75°C

OPERATING CHARACTERISTICS

Clock fall time ≤ 150 ns.

Triggers on clock pulse widths ≥ 20 ns.

Provides direct $\overline{\text{SET}}$, $\overline{\text{PRESET}}$, and $\overline{\text{RESET}}$ inputs. The application of a "0" state to 8 or 9, sets Q high; "0" state to 13, resets Q low. The clock must be in the low state when these functions are performed.

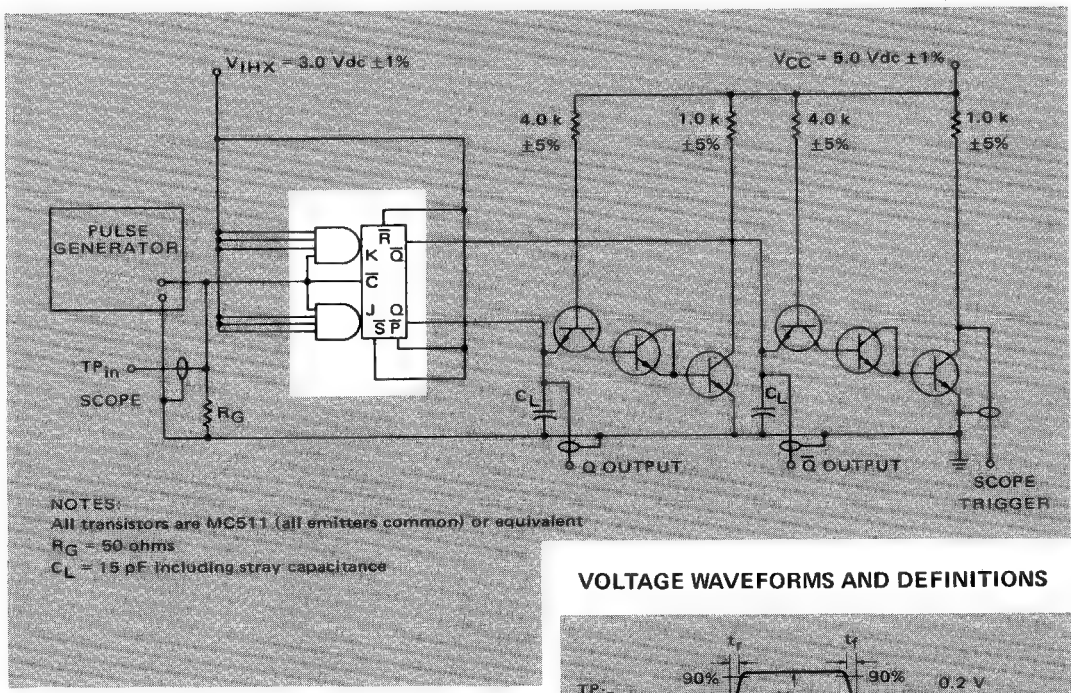
Data at the J and K inputs must be present before the clock goes to a high state. If the information on the J and K inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1"

state to "0" state information change on the J and K terminals. The flip-flop will require typically 10 ns to recognize a "0" state to "1" state change.

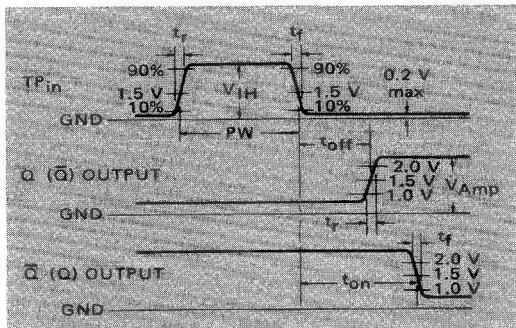
Negative edge triggering – When the clock goes from the high state to the low state, the information in the temporary storage section is transferred and the Q and $\overline{\text{Q}}$ outputs will respond accordingly. While the clock is in a low state, the J and K terminals are inhibited.

Unused J and K inputs should be tied to the clock or to 2.0 to 5.0 Vdc. $\overline{\text{PRESET}}$ and $\overline{\text{SET}}$ are tied to $\overline{\text{Q}}$; $\overline{\text{RESET}}$ is tied to Q.

FIGURE 1 – SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



VOLTAGE WAVEFORMS AND DEFINITIONS



SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	t_{off}	V		20	ns
Delay Time On	t_{on}	V		40	ns
Rise Time	t_r	V		8.0	ns
Fall Time	t_f	V		5.0	ns
Amplitude	V_{Amp}	V	3.2		Volt

WORST-CASE TESTS

(Device must toggle with each clock pulse)

TEST	SYMBOL	LIMITS	INPUT CONDITIONS
Toggle Frequency	f_{Tog}	20 MHz max	W
Pulse Width	PW	20 ns min	X
Input High Voltage	V_{IH}	1.8 V min	Y
Fall Time	t_f	150 ns max	Z

INPUT PULSE CONDITIONS

SYMBOL	W	V	X	Y	Z	UNIT
PRF	20	5.0	5.0	5.0	1.0	MHz
PW	20	100	20	100	200	ns
t_r	≤ 10	≤ 10	≤ 10	≤ 10	≤ 50	ns
t_f	≤ 10	≤ 10	≤ 10	≤ 10	150	ns
V_{IH}	3.5	3.5	3.5	1.8	3.5	Volt

FIGURE 2 – J-K TERMINAL CHARACTERISTICS TEST CIRCUIT

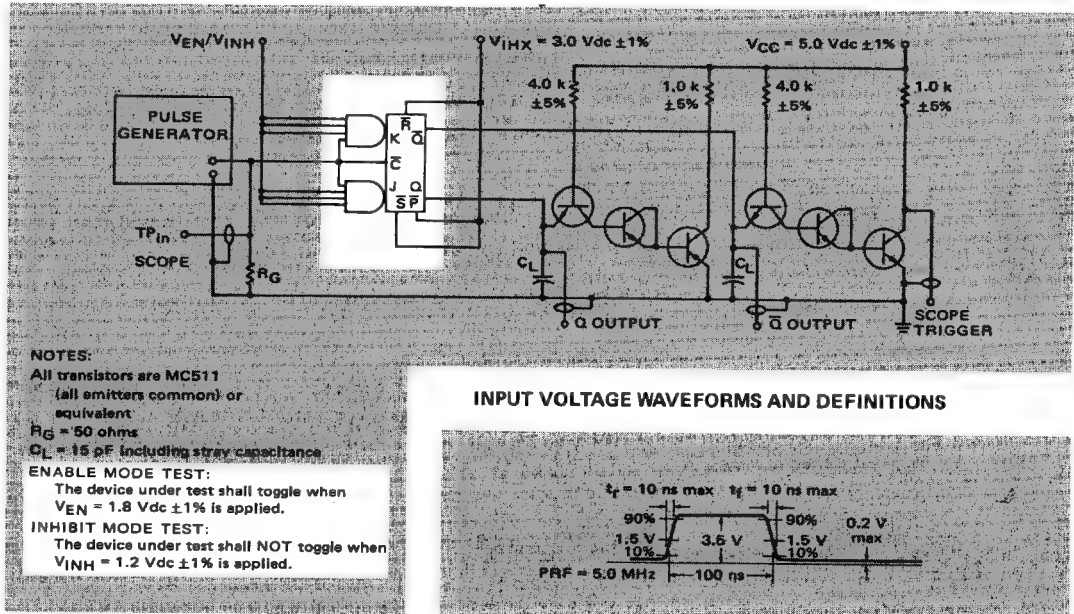
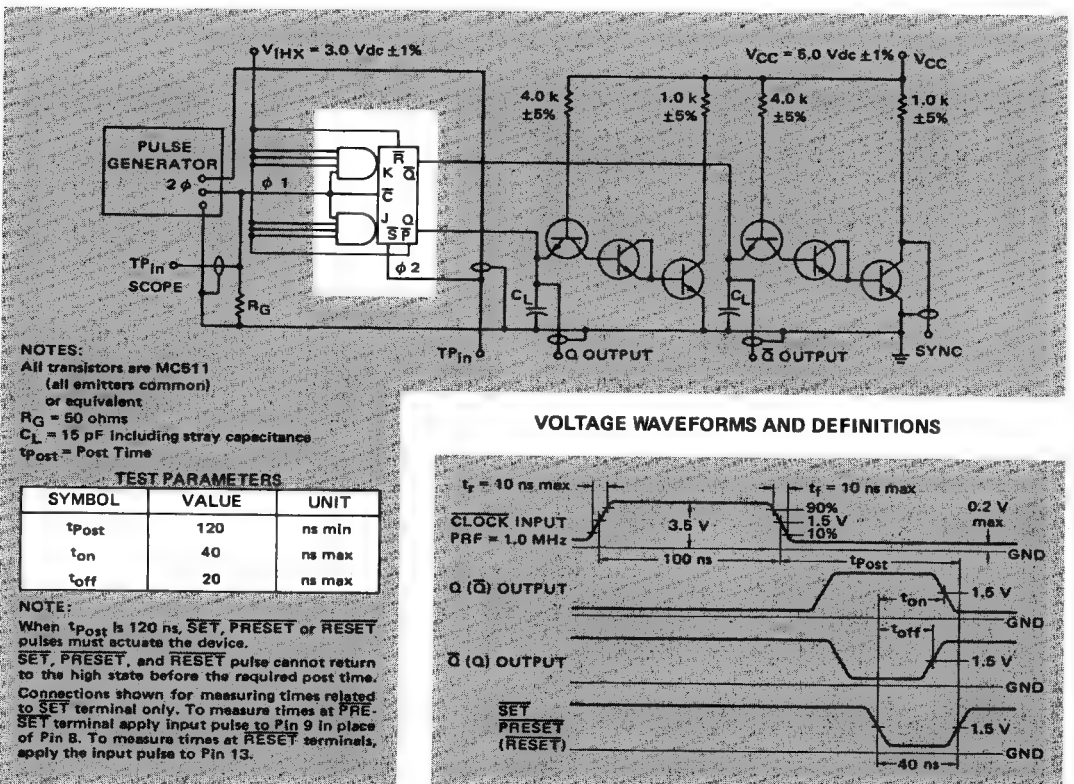
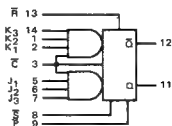


FIGURE 3 – SET-RESET-PRESET TERMINAL CHARACTERISTICS TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (continued)

Test procedures are shown for only one J and K input, plus the SET, PRESET, and RESET inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



MC515*, MC565

MC415*, MC465

@ Test Temperature

-55°C

+25°C

+125°C

0°C

+25°C

+75°C

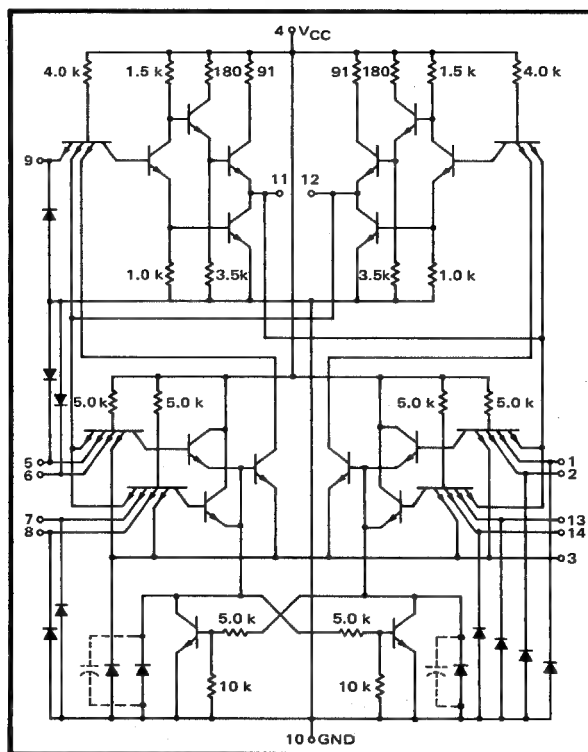
TEST CONDITIONS														TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:										Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:										Gnd
mA						Volts																													
I _{OL}		I _{OH}		I _{in}	2 I _{in}	V _{IL}	V _{IH}	V _R	V _{th0}	V _{th1}	V _{out}	V _{CC}																							
Pr*	Std	Pr*	Std																																
20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.0	2.0	5.5	5.0																							
20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.2	1.7	5.5	5.0																							
20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	0.9	1.4	5.5	5.0																							
20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.9	5.5	5.0																							
20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.2	1.8	5.5	5.0																							
20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.7	5.5	5.0																							
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																																			
I _{OL}	I _{OH}	I _{in}	2 I _{in}	V _{IL}	V _{IH}	V _R	V _{th0}	V _{th1}	V _{out}	V _{CC}				Gnd																					
-	-	-	-	-	-	1,2,5,6, 7,8,9,13,14	-	-	-	4				3,10																					
-	-	-	-	-	-	3	-	-	-	4				1,2,5,6,7,10,14																					
-	-	-	-	13	-	3	-	-	-	4				10																					
-	-	-	-	8	-	3	-	-	-	4				10																					
-	-	-	3	13	-	-	-	-	-	4				10																					
-	-	-	3	8	-	-	-	-	-	4				10																					
-	-	-	3	-	-	-	-	-	-	4				1,2,5,6,7,10,14																					
12	-	-	-	-	-	-	-	13	-	4				3,8,10																					
11	-	-	-	-	-	-	-	9	-	4				3,10,13																					
11	-	-	-	-	-	-	-	8	-	4				3,10,13																					
-	12	-	-	-	-	-	-	13	-	4				8,10																					
-	11	-	-	-	-	-	-	9	-	4				10,13																					
-	11	-	-	-	-	-	-	8	-	4				10,13																					
-	-	-	-	-	-	-	-	-	12	4				1,2,3,5,6,7,8,9,10,13,14																					
-	-	-	-	-	-	-	-	-	11	4				1,2,3,5,6,7,8,9,10,13,14																					
-	-	-	-	-	-	-	-	-	-	4				1,2,3,5,6,7,8,9,10,12,13,14																					
-	-	-	-	-	-	-	-	-	-	4				1,2,3,5,6,7,8,9,10,11,13,14																					
12	-	-	-	-	13	-	-	-	-	4				3,8,10																					
11	-	-	-	-	9	-	-	-	-	4				3,10,13																					
11	-	-	-	-	8	-	-	-	-	4				3,10,13																					
-	12	-	-	-	13	-	-	-	-	4				8,10																					
-	11	-	-	-	9	-	-	-	-	4				10,13																					
-	11	-	-	-	8	-	-	-	-	4				10,13																					
-	-	-	-	-	-	-	-	-	-	4				3,10,13																					
-	-	-	-	-	-	-	-	-	-	4				3,8,10																					

* Prime Fan-Out.

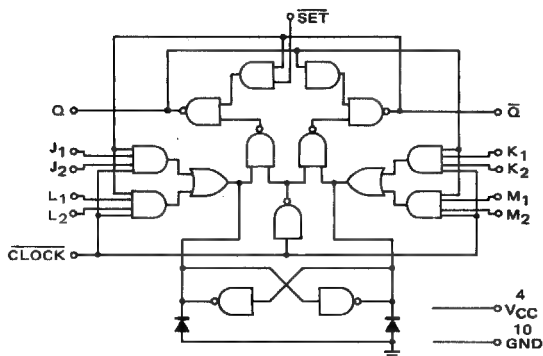
"OR" J-K FLIP-FLOP

MTTL MC500/400 series

MC516 • MC566 MC416 • MC466



EQUIVALENT CIRCUIT

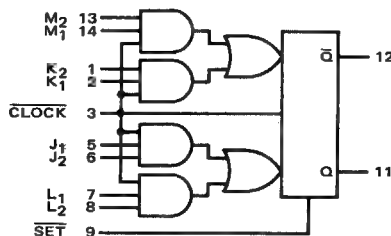


The MC516, MC566, MC416, and MC466 are clocked flip-flops that trigger on the negative edge and are internally wired to perform the J-K logic function. Each flip-flop has a positive logic AND-OR input gating configuration that consists of two clocked J inputs ANDed together, two clocked K inputs ANDed together, two clocked L inputs ANDed together, and two clocked M inputs ANDed together. The J and the L inputs are ORed together and the K and the M inputs are ORed together. A direct SET is also available.

In normal operation, information is changed on the clocked inputs while the clock is in a low state, since the inputs are inhibited in this condition. Information is read into a temporary memory through the AND-OR input gating when the clock is in the high state. When the clock returns low the information in the temporary memory is transferred to the bi-stable section and the Q and the \bar{Q} outputs respond accordingly. The information on the clocked inputs should not be changed while the clock is high.

Each flip-flop can be set directly by applying a low state to the direct SET input. Since each flip-flop is a charge storage device there is a restriction on the clock fall time that must be observed.

The AND-OR input configuration of each flip-flop makes it very useful for shift right/shift left registers and for up/down counters.



J	L	K	M	Q_n	Q_{n+1}
0	0	X	X	0	0
1	X	X	X	0	1
X	1	X	X	0	1
X	X	0	0	1	1
X	X	1	X	1	0
X	X	X	1	1	0

X = Don't Care
Where $J = J_1 \cdot J_2$
 $L = L_1 \cdot L_2$
 $K = K_1 \cdot K_2$
 $M = M_1 \cdot M_2$

Total Power Dissipation = 60 mW typ/ pkg

Switching Times:

$t_{on} = 25$ ns typ

$t_{off} = 13$ ns typ

SERIES	INPUT LOADING FACTOR (If)				OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
	CLOCK	ALL OTHER	CLOCK	ALL OTHER		
MC516 MC566	3	1	(-4.0 mA)	(-1.33 mA)	15 MC500 series Gates (20 mA) 7 MC500 series Gates (10 mA)	-55°C to +125°C
MC416 MC466	3	1	(-5.0 mA)	(-1.66 mA)	12 MC400 series Gates (20 mA) 6 MC400 series Gates (10 mA)	0°C to +75°C

OPERATING CHARACTERISTICS

Clock fall time ≤ 150 ns.

Triggers on clock pulse widths ≥ 20 ns.

The application of a "0" state to the $\overline{\text{SET}}$ will cause Q to go to the "1" state. The clock must be in the low state when this function is performed.

Data at the clocked inputs must be present before the clock goes to a high state. If the information on the clocked inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1" state to "0" state change. The flip-flop will also require typically 10 ns to recognize a "0" state to "1" state change.

Negative edge triggering – When the clock goes from the high

state, the information in the temporary storage section is transferred; and the Q and $\overline{\text{Q}}$ outputs will change accordingly. While the clock is in a low state, the J, K, L, and M terminals are inhibited.

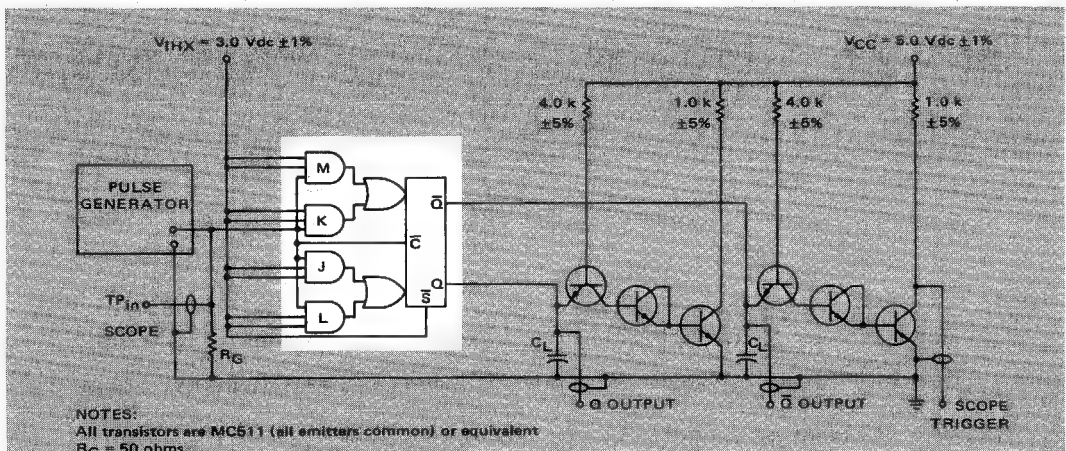
Unused Inputs:

Single unused J, K, L, and M inputs should be tied to the used input, to the clock input, or to 2.0 to 5.0 Vdc.

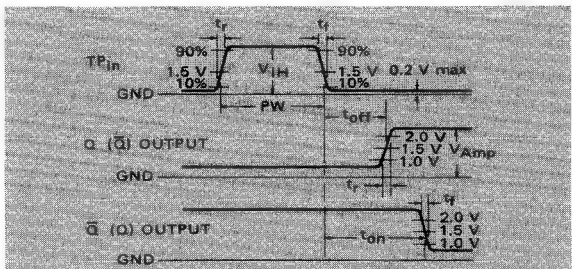
If both J, K, L, or M inputs are unused, they MUST be tied to ground.

Unused $\overline{\text{SET}}$ is tied to $\overline{\text{Q}}$.

FIGURE 1 – SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



VOLTAGE WAVEFORMS AND DEFINITIONS



SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	t_{off}	V		20	ns
Delay Time On	t_{on}	V		40	ns
Rise Time	t_r	V		8.0	ns
Fall Time	t_f	V		5.0	ns
Amplitude	V _{Amp}	V	3.2		Volt
WORST-CASE TESTS (Device must toggle with each clock pulse)					
TEST	SYMBOL	LIMITS	INPUT CONDITIONS		
Toggle Frequency	f_{Tog}	20 MHz max	W		
Pulse Width	PW	20 ns min	X		
Input High Voltage	V_{IH}	1.8 V min	Y		
Fall Time	t_f	150 ns max	Z		

INPUT PULSE CONDITIONS						
SYMBOL	W	V	X	Y	Z	UNIT
PRF	20	5.0	5.0	5.0	1.0	MHz
PW	20	100	20	100	200	ns
t_r	≤ 10	≤ 10	≤ 10	≤ 10	≤ 50	ns
t_f	≤ 10	≤ 10	≤ 10	≤ 10	≤ 150	ns
V_{IH}	3.5	3.5	3.5	1.8	3.5	Volt

MC516, MC566/MC416, MC466 (continued)

FIGURE 2 – J-K-L-M TERMINAL CHARACTERISTICS TEST CIRCUIT

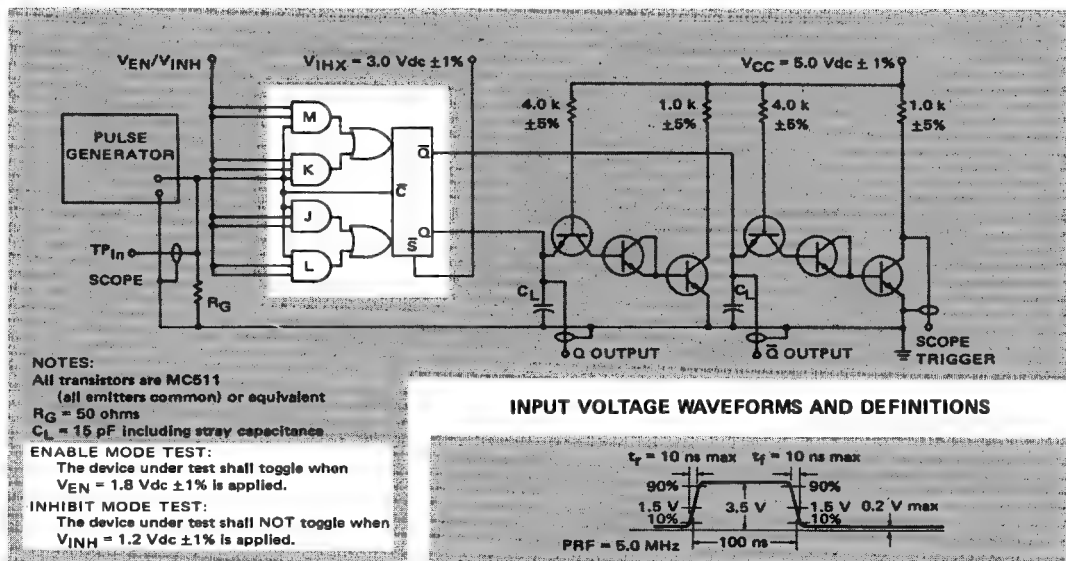
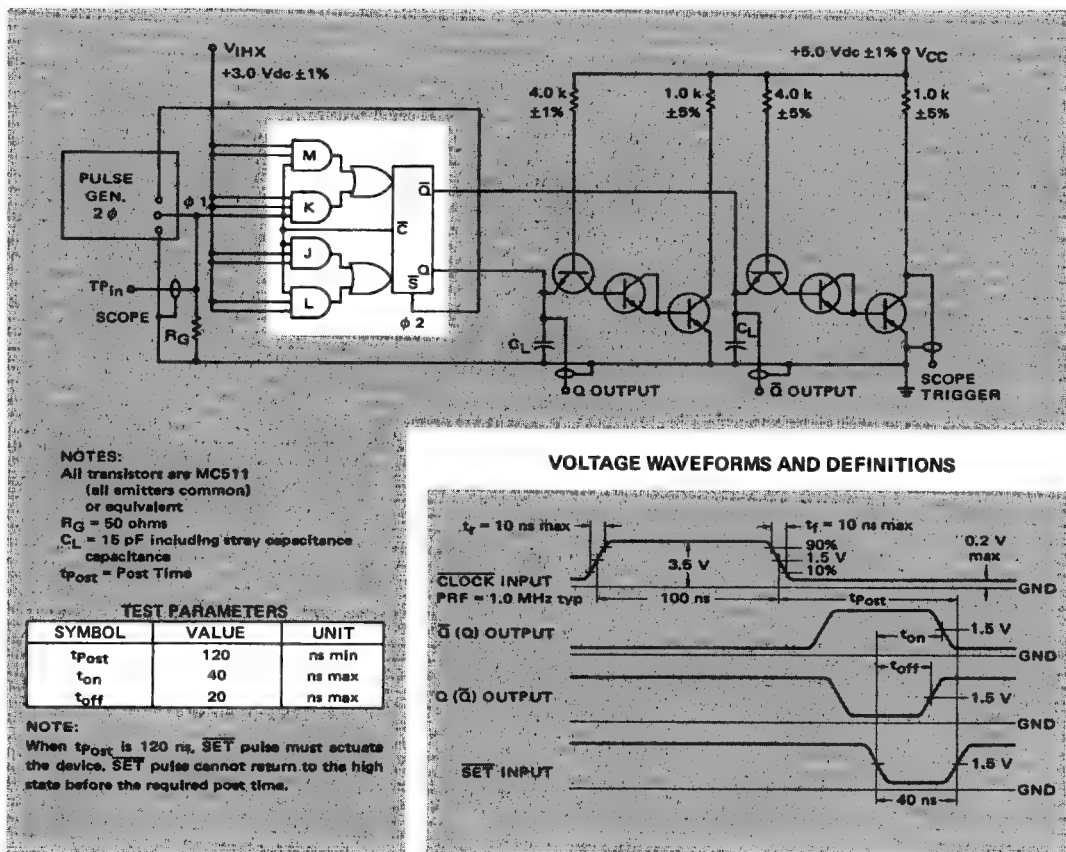
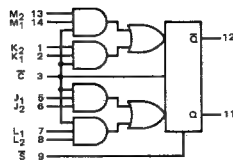


FIGURE 3 – SET TERMINAL CHARACTERISTICS TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J, one K, and the SET input. The remaining J, K, L, M inputs are tested in the same manner.



@ Test
Temperature

MC516*, MC566

-55°C

+25°C

+125°C

MC416*, MC466

0°C

+25°C

+75°C

TEST CONDITIONS															
mA								Volts							
I_{OL}	I_{OH}	I_{in}	$2 I_{in}$	$4 I_{in}$	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{CC}				
Pr*	Std	Pr*	Std												
20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0		
20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0		
20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0		
20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0		
20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0		
20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0		

TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:															
I_{OL}	I_{OH}	I_{in}	$2 I_{in}$	$4 I_{in}$	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{CC}	Gnd			
-	-	-	-	-	-	-	2,3,5,6,7,8,13,14	-	-	-	4	1,9,10			
-	-	-	-	-	-	-	1,2,3,6,7,8,13,14	-	-	-	↓	5,10,11			
-	-	-	-	-	-	-	1,2,5,6,7,8,13,14	-	-	-	↓	3,9,10,11			
-	-	-	-	-	-	-	1	-	-	-	4	2,3,5,6,7,8,10,11,13,14			
-	-	-	-	-	-	-	5	-	-	-	↓	1,2,3,6,7,8,9,10,12,13,14			
-	-	-	-	-	-	-	9	-	-	-	↓	1,2,3,5,6,7,8,10,12,13,14			
-	-	-	-	-	-	-	1	-	-	-	4	9,10			
-	-	-	-	-	-	-	5	-	-	-	↓	10,11			
-	-	-	-	-	-	-	9	-	-	-	↓	10,11			
-	-	1	-	-	-	-	-	-	-	-	4	9,10			
-	-	5	-	-	-	-	-	-	-	-	↓	10,11			
-	-	9	-	-	-	-	-	-	-	-	↓	10,11			
-	-	1	-	-	-	-	-	-	-	-	4	2,3,5,6,7,8,10,11,13,14			
-	-	5	-	-	-	-	-	-	-	-	↓	1,2,3,6,7,8,9,10,12,13,14			
-	-	9	-	-	-	-	-	-	-	-	↓	1,2,3,5,6,7,8,10,12,13,14			

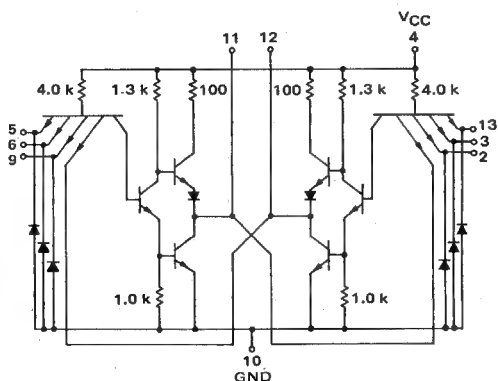
* Prime Fan-Out

① Momentarily ground pin prior to taking measurement at terminal.

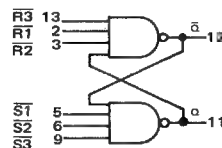
R-S FLIP-FLOP

MTTL MC500/400 series

MC513 · MC563
MC413 · MC463



This device consists of two independent dual 4-input NAND gates, internally cross coupled to realize a multiple input R-S flip-flop. The circuit can be used to eliminate switch contact bounce and to provide a temporary storage for data.



$$\bar{R} = 2 \cdot 3 \cdot 13$$

$$\bar{S} = 5 \cdot 6 \cdot 9$$

Positive Logic =

$$11 = Q = \bar{S} + \bar{6} + \bar{9} + \bar{12}$$

Total Power Dissipation = 30 mW typ/pkg
Propagation Delay Time = 20 ns typ (to change state)

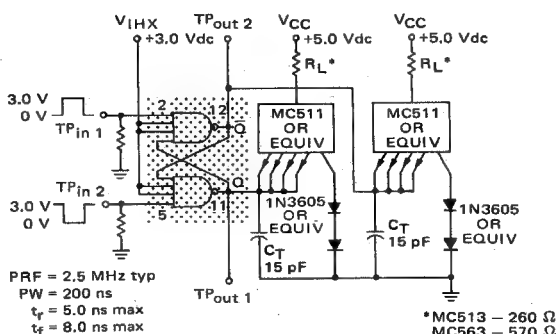
TRUTH TABLE (Positive Logic)

\bar{R}	\bar{S}	Q	\bar{Q}
0	0	Not Permitted	
0	1	0	1
1	0	1	0
1	1	Q	\bar{Q}

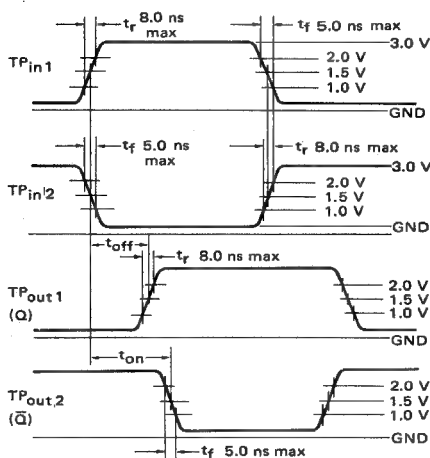
SERIES	INPUT LOADING FACTOR (I_{IF})	OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
MC513 MC563	1 (-1.33 mA)	15 7 MC500 series Gates (20 mA) MC500 series Gates (10 mA)	-55°C to +125°C
MC413 MC463	1 (-1.66 mA)	12 6 MC400 series Gates (20 mA) MC400 series Gates (10 mA)	0°C to +75°C

SWITCHING TIME TEST CIRCUIT †

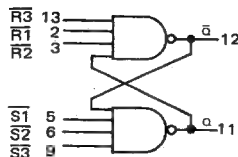
VOLTAGE WAVEFORMS AND DEFINITIONS



NOTES: $R_G = 50$ ohms
 C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
† To measure t_{on} , t_r for Q and t_{off} , t_f for \bar{Q} , reverse input polarities.



Test procedures are shown for only one input. The other inputs are tested in the same manner.



MC513*, MC563

MC413*, MC463

[illegible]

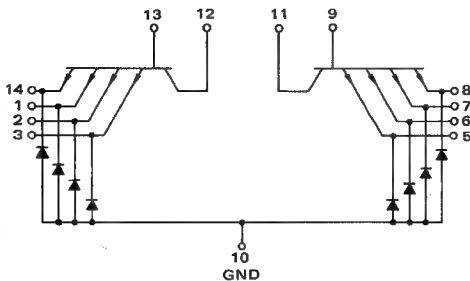
† To measure t_{on} , t_f for Q and t_{off} , t_r for \bar{Q} , reverse input polarities.

MC513, MC563/MC413, MC463 (continued)

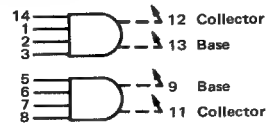
DUAL 4-INPUT EXPANDER FOR "NAND" GATES

MTTL MC500/400 series

MC511 • MC561
MC411 • MC461



This device consists of two independent 4-emitter input transistors, each of which performs the positive logic AND function when used in conjunction with expandable gates. The base and collector of each device is available for expansion. Using the MC511 with the MC506 expandable gate, the number of AND inputs can be expanded to 20.



Total Power Dissipation = 0 mW typ/pkg

Propagation Delay Time:

$\Delta t_{pd} = +3.0$ ns typ

When added to the expandable "AND-OR-INVERT" gate.

$\Delta t_{pd}/pF = +1.6$ ns/pF typ

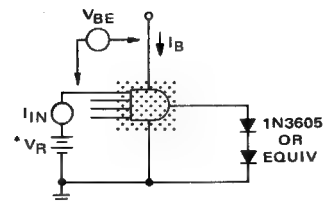
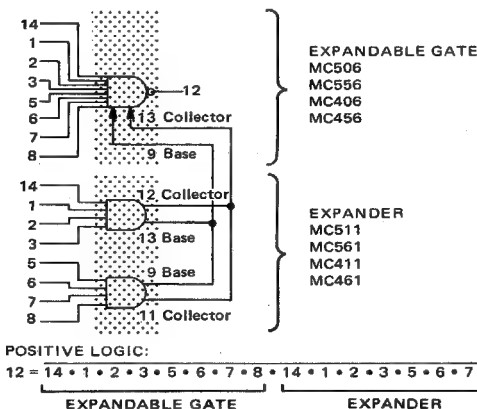
Caused by additional capacitance at expander points.

SERIES	INPUT LOADING FACTOR	(I_F)	TEMPERATURE RANGE
MC511 MC561	1	(-1.33 mA)	-55°C to +125°C
MC411 MC461	1	(-1.66 mA)	0°C to +75°C

Full output loading factor of the expandable gate is maintained.

APPLICATION: EXPANDABLE 8-INPUT "AND-OR-INVERT" GATE WITH A DUAL 4-INPUT EXPANDER CONNECTED.

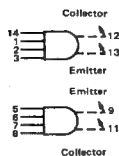
BV_{in} "0", V_{BE} , I_L TEST CIRCUIT



* $V_R = 0$ V for V_{BE} test

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



MC511 , MC561		MC411 , MC461	MC461 Test Limits	TEST CONDITIONS										Gnd †
				mA			Volts							
				I _{B1}	I _{B2}	I _{in}	V _R	V _{DC}	V _C					
@ Test Temperature				-55°C	1.33	1.0	1.0	4.5	**	1.5				
				+25°C	1.33	1.0	1.0	4.5	**	1.5				
				+125°C	1.33	1.0	1.0	4.5	**	1.5				
				0°C	1.66	1.0	1.0	4.5	**	1.5				
				+25°C	1.66	1.0	1.0	4.5	**	1.5				
				+75°C	1.66	1.0	1.0	4.5	**	1.5				
				TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:										
				I _{B1}	I _{B2}	I _{in}	V _R	V _{DC}	V _C					
				Min	Max	Min	Max	Unit						
-	100	-	100	μAdc	13	-	-	1	-	-	2,3,10,14			
-	100	-	100	μAdc	-	13	-	1	12	-	10			
5.5	-	5.5	-	Vdc	-	13	1	-	12	-	10			
5.5	-	5.5	-	Vdc	13	-	1	-	-	-	2,3,10,14			
-	1.2	-	1.1	Vdc	13	-	-	-	12	-	1,10			
-	1.2	-	1.1	Vdc	-	13	-	-	-	-	10,12			
-	0.2	-	0.2	Vdc	13	-	-	-	-	-	1,10			
3.0	-	3.0	-	-	13	-	-	-	-	12 ‡	1,10			

† Ground inputs to expanders not under tests during ALL tests

* Measure V_O from Pin 12 to gnd

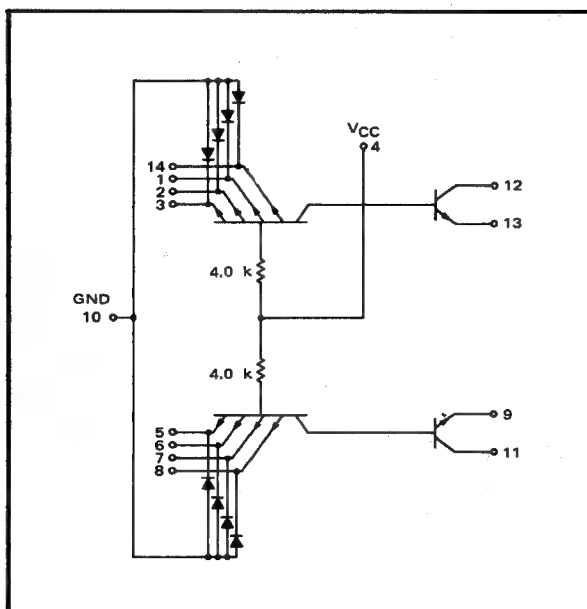
** Voltage obtained with two series diodes tied from collector to gnd.

‡ Measure I_C and calculate Beta. $(h_{FE} = \frac{I_C}{I_B})$

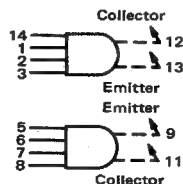
DUAL 4-INPUT EXPANDER FOR "AND-OR-INVERT" GATES

MTTL MC500/400 series

MC510 • MC560
MC410 • MC460



This device consists of two independent 4-input AND gates. The outputs of each gate are made available as ORing nodes. Using the MC509 series and the MC510 series with any one of the basic expandable gates, up to 10 AND gates can be ORed together.



Total Power Dissipation = 10 mW typ/Pkg.

Propagation Delay Time:

$\Delta t_{pd} = +1.0$ ns typ

When added to the expandable "AND-OR-INVERT" gate.

$\Delta t_{pd}/pF = +1.0$ ns/pF typ

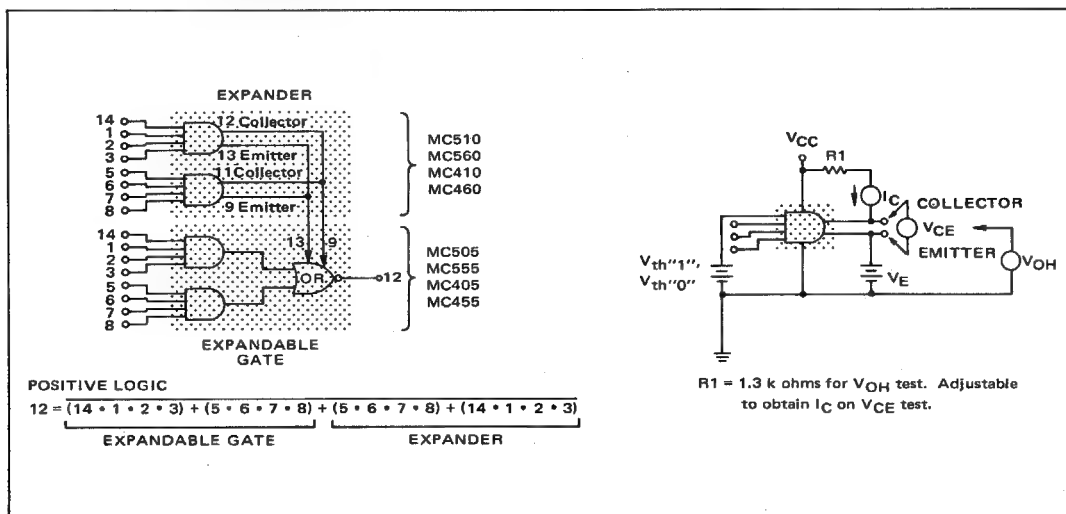
Caused by additional capacitance at expansion points.

SERIES	INPUT LOADING FACTOR (I_F)	TEMPERATURE RANGE
MC510 MC560	1 (-1.33 mA)	-55°C to +125°C
MC410 MC460	1 (-1.66 mA)	0°C to +75°C

Full output loading factor of the expandable gate is maintained.

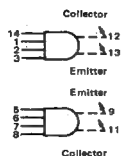
APPLICATION: EXPANDABLE 2-WIDE 4-INPUT, "AND-OR-INVERT" GATE WITH A DUAL 4-INPUT EXPANDER CONNECTED.

VCE, VOH TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



MC510, MC560

MC410, MC460

@ Test
Temperature

-55°C
 +25°C
 +125°C
 0°C
 +25°C
 +75°C

TEST CONDITIONS														
mA		Volts												
I _C	I _{in}	V _R	V _{E1}	V _{E2}	V _{E3}	V _{th1}	V _{th0}	V _{out}	V _{CR}	V _{CRH}	V _{CC}	V _{CCH}		
4.0	1.0	4.5	1.00	0.90	0.8	2.0	1.0	5.5	*	-	5.0	-		
4.0	1.0	4.5	0.85	0.75	0.8	1.7	1.2	5.5	*	**	5.0	8.0		
4.0	1.0	4.5	0.65	0.55	0.8	1.4	0.9	5.5	*	-	5.0	-		
4.0	1.0	4.5	0.90	0.80	0.8	1.9	1.1	5.5	*	-	5.0	-		
4.0	1.0	4.5	0.85	0.75	0.8	1.8	1.2	5.5	*	**	5.0	7.0		
4.0	1.0	4.5	0.75	0.65	0.8	1.7	1.1	5.5	*	-	5.0	-		
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:														
I _C	I _{in}	V _R	V _{E1}	V _{E2}	V _{E3}	V _{th1}	V _{th0}	V _{out}	V _{CR}	V _{CRH}	V _{CC}	V _{CCH}	Gnd†	
-	-	2,3,14	-	-	-	-	-	-	-	-	4	-	1,10	
-	-	1	-	-	-	-	-	-	-	-	4	-	2,3,10,14	
-	-	1	13	-	-	-	-	-	12	-	4	-	10	
-	1	-	13	-	-	-	-	-	12	-	4	-	10	
-	1	-	-	-	-	-	-	-	-	-	4	-	2,3,10,14	
-	-	-	-	13	-	-	1	-	12	-	4	-	10	
12	-	-	13	-	-	1	-	-	-	-	4	-	10	
-	-	-	-	-	13	-	-	12	-	-	4	-	1,2,3,10,14	
-	-	-	-	-	9,13	-	-	-	-	11, 12	-	4	1,2,3,10,14	
-	-	-	-	-	9,13	-	-	-	-	-	4	-	10†	
-	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,10,14	

* Indicated pins tied to V_{CC} thru 1.3 k ohms ± 1.0% resistor.

** Indicated pins tied to V_{CCH} thru 1.3 k ohms ± 1.0% resistor.

† Ground inputs to gate not under test during ALL tests, unless otherwise noted.

‡ The inputs of both gates must be ungrounded.

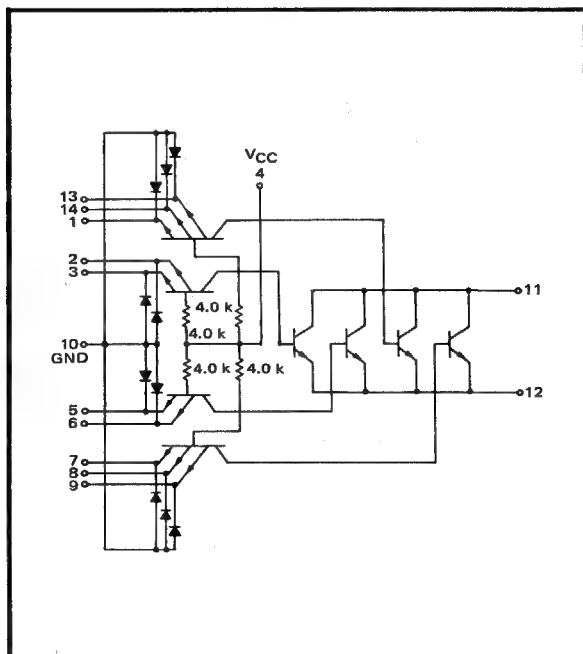
① V_{CE} is referenced to the emitter voltage (Pin 13). The other gate is referenced to (Pin 9).

② Pin 9 ties to Pin 13. Pin 12 ties to Pin 11.

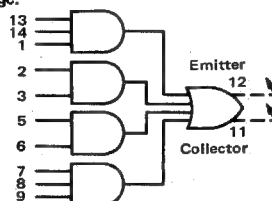
4-WIDE 3-2-2-3 INPUT EXPANDER FOR "AND-OR-INVERT" GATES

MTTL MC500/400 series

MC509 • MC559
MC409 • MC459



This device consists of two 2-input and two 3-input AND gates ORed together with the common ORing nodes made available as the output. The basic expandable gate can be expanded up to 10 AND gates by using the MC509 series or the MC510 series expander package.



Total Power Dissipation = 20 mW/pkg.

Propagation Delay Time:

$\Delta t_{pd} = +4.0$ ns typ (1.0 ns per ORed function)
When added to the expandable "AND-OR-INVERT" gate.

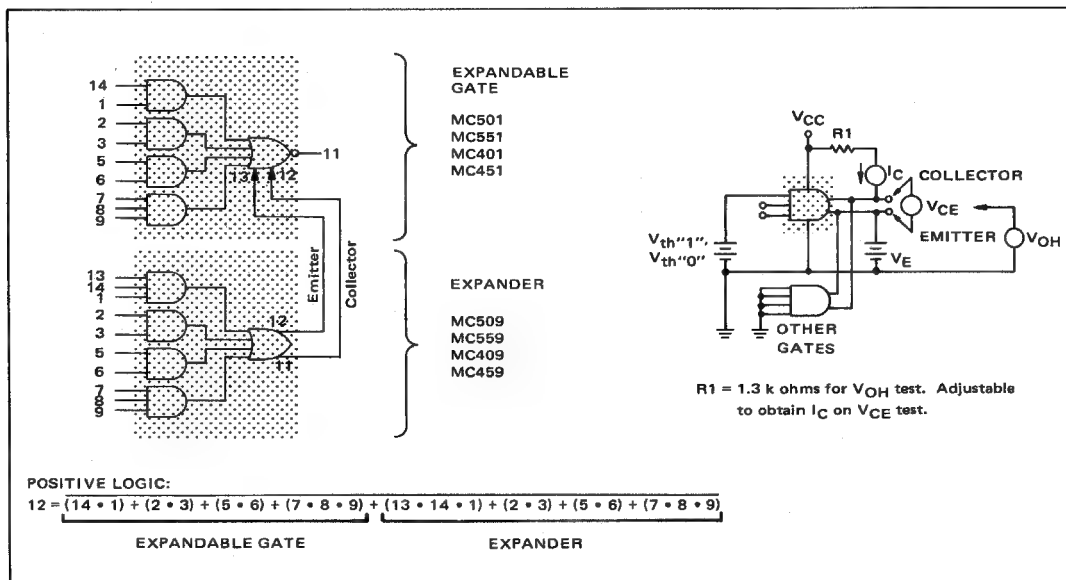
$\Delta t_{pd}/pF = 1.0$ ns/pF typ
Caused by additional capacitance at expansion points.

SERIES	INPUT LOADING FACTOR (I_F)	TEMPERATURE RANGE
MC509 MC559	1 (-1.33 mA)	-55°C to +125°C
MC409 MC459	1 (-1.66 mA)	0°C to +75°C

Full output loading factor of the expandable gate is maintained.

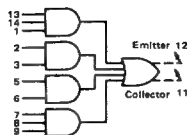
APPLICATION: EXPANDABLE 4-WIDE "AND-OR-INVERT" GATE WITH A 4-WIDE 3-2-2-3 INPUT EXPANDER CONNECTED.

V_{CE} , V_{OH} TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.



MC509, MC559

MC409, MC459

@ Test
Temperature

-55°C
 +25°C
 +125°C
 0°C
 +25°C
 +75°C

TEST CONDITIONS															Gnd
mA		Volts													
I _C	I _{In}	V _R	V _{E1}	V _{E2}	V _{E3}	V _{th1}	V _{th0}	V _{out}	V _{CR}	V _{CRH}	V _{CC}	V _{CCH}			
4.0	1.0	4.5	1.00	0.90	0.8	2.0	1.0	5.5	*	-	5.0	-			
4.0	1.0	4.5	0.85	0.75	0.8	1.7	1.2	5.5	*	**	5.0	8.0			
4.0	1.0	4.5	0.65	0.55	0.8	1.4	0.9	5.5	*	-	5.0	-			
4.0	1.0	4.5	0.90	0.80	0.8	1.9	1.1	5.5	*	-	5.0	-			
4.0	1.0	4.5	0.85	0.75	0.8	1.8	1.2	5.5	*	**	5.0	7.0			
4.0	1.0	4.5	0.75	0.65	0.8	1.7	1.1	5.5	*	-	5.0	-			
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:															
I _C	I _{In}	V _R	V _{E1}	V _{E2}	V _{E3}	V _{th1}	V _{th0}	V _{out}	V _{CR}	V _{CRH}	V _{CC}	V _{CCH}	Gnd		
c	-	-	2,3,5,6,7,8,9,13,14	-	-	-	-	-	-	-	4	-	1,10		
c	-	-	1	-	-	-	-	-	-	-	4	-	2,3,5,6,7,8,9,10,13,14		
c	-	-	1	12	-	-	-	-	11	-	4	-	2,3,5,6,7,8,9,10		
	-	1	-	12	-	-	-	-	11	-	4	-	2,3,5,6,7,8,9,10		
	-	1	-	-	-	-	-	-	-	-	4	-	2,3,5,6,7,8,9,10,13,14		
	-	-	-	12	-	-	1	-	11	-	4	-	2,3,5,6,7,8,9,10		
	11	-	-	12	-	-	1	-	-	-	4	-	2,3,5,6,7,8,9,10		
e	-	-	-	-	-	12	-	-	11	-	4	-	1,2,3,5,6,7,8,9,10,13,14		
	-	-	-	-	-	12	-	-	-	-	11	-	4	1,2,3,5,6,7,8,9,10,13,14	
c	-	-	-	-	-	12	-	-	-	-	4	-	10		
c	-	-	-	-	-	12	-	-	-	-	4	-	1,2,3,5,6,7,8,9,10,13,14		

* Indicated pins tied to V_{CC} thru 1.3 kohms ± 1.0% resistor.

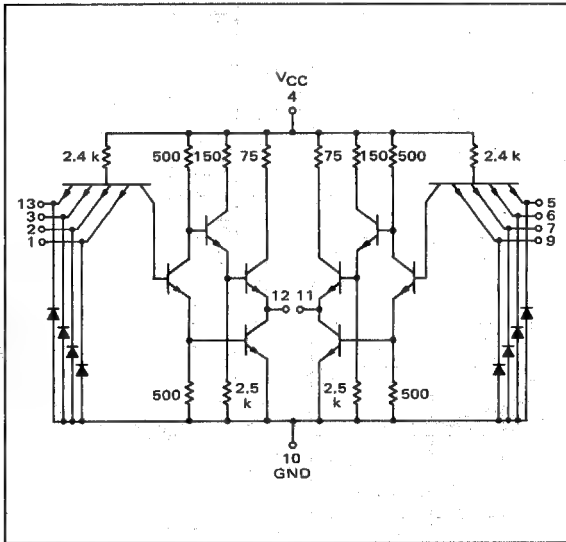
** Indicated pins tied to V_{CCH} thru 1.3 kohms ± 1.0% resistor.

① V_{CE} is referenced to the emitter Voltage (Pin 12).

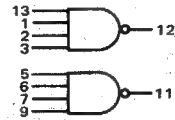
DUAL 4-INPUT LINE DRIVER

MTTL MC500/400 series

MC507 • MC557 MC407 • MC457



Each of the two independent drivers in the package consists of a 4-input AND gate driving an output inverter. The output inverter is capable of supplying twice the drive of the basic gates. The line driver is especially useful for driving high capacitive loads or for driving large fan-outs such as the numerous clock inputs of large counters.



Positive Logic:
 $12 = 1 \cdot 2 \cdot 3 \cdot 13$

Negative Logic:
 $12 = 1 + 2 + 3 + 13$

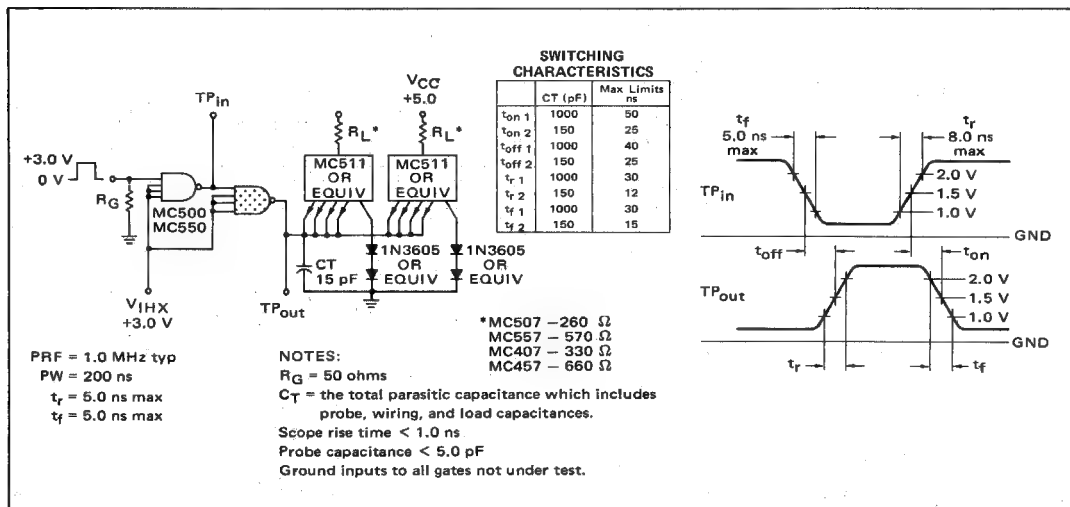
Total Power Dissipation = 60 mW typ/pkg
Propagation Delay Time = 25 ns typ @ 1000 pF Load

SERIES	INPUT LOADING FACTOR (I_F)	OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
MC507 MC557	1.5 (-2.0 mA)*	30 MC500 series Gates (40 mA) 15 MC500 series Gates (20 mA)	-55°C to +125°C
MC407 MC457	1.5 (-2.5 mA)*	24 MC400 series Gates (40 mA) 12 MC400 series Gates (20 mA)	0°C to +75°C

*Use I_F value of gate being driven (-1.33 or -1.66) to calculate output drive capability of line driver.

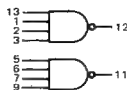
SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one device. The other device is tested in the same manner. Further, test procedures are shown for only one input of the device under test. To complete testing, sequence through remaining inputs.



MC507*, MC557

MC407*, MC457

@ Test Temperature

-55°C
+25°C
+125°C
0°C
+25°C
+75°C

														TEST CONDITIONS														Gnd †
mA														Volts														
I _{OL}		I _{OH}		I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out1}	V _{out2}	V _{OL}	V _{CC}	V _{CCH}	V _{IHX}													
Pr*	Std	Pr*	Std																									
C	40	20	-3.0	-1.5	1.0	0.45	2.8	4.5	2.0	1.0	5.5	-	-	5.0	-	-												
C	40	20	-3.0	-1.5	1.0	0.45	2.8	4.5	1.7	1.2	5.5	6.5	8.0	5.0	8.0	3.0												
C	40	20	-3.0	-1.5	1.0	0.45	2.8	4.5	1.4	0.9	5.5	-	-	5.0	-	-												
C	40	20	-2.4	-1.2	1.0	0.45	3.0	4.5	1.9	1.1	5.5	-	-	5.0	-	-												
C	40	20	-2.4	-1.2	1.0	0.45	3.0	4.5	1.8	1.2	5.5	6.5	8.0	5.0	7.0	3.0												
C	40	20	-2.4	-1.2	1.0	0.45	3.0	4.5	1.7	1.1	5.5	-	-	5.0	-	-												
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																												
I _{OL}		I _{OH}		I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out1}	V _{out2}	V _{OL}	V _{CC}	V _{CCH}	V _{IHX}													
																	Gnd †											
c	-	-	-	-	-	-	2,3,13	-	-	-	-	-	4	-	-	1,10												
c	-	-	-	-	-	-	1	-	-	-	-	-	4	-	-	2,3,10,13												
c	-	-	-	-	-	-	1	-	-	-	-	-	4	-	-	10												
	-	-	1	-	-	-	-	-	-	-	-	-	4	-	-	10												
	-	-	1	-	-	-	-	-	-	-	-	-	4	-	-	2,3,10,13												
	12	-	-	-	-	-	-	1	-	-	-	-	4	-	-	10												
	-	12	-	-	-	-	-	-	1	-	-	-	4	-	-	10												
c	-	-	-	-	-	-	-	-	-	-	-	-	12	4	-	10												
c	-	-	-	-	-	-	-	-	-	-	-	-	12	4	-	10												
c	-	-	-	-	-	-	-	-	-	-	12	-	4	-	-	1,2,3,10,13												
c	-	-	-	-	-	-	-	-	-	12	-	-	4	-	-	1,2,3,10,13												
c	-	-	-	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,10,12,13												
	-	12	-	1	-	-	-	-	-	-	-	-	4	-	-	10												
	12	-	-	-	1	-	-	-	-	-	-	-	4	-	-	10												
c	-	-	-	-	-	-	-	-	-	-	-	-	-	4	-	1,5,10												
c	-	-	-	-	-	-	-	-	-	-	-	-	4	-	-	10†												
c	-	-	-	-	-	-	-	-	-	-	-	-	4	-	-	1,5,10												
Pulse In		Pulse Out																										
	1	12	-	-	-	-	-	-	-	-	-	-	4	-	2,3,13	10												
	1	12	-	-	-	-	-	-	-	-	-	-	4	-	2,3,13	10												
	1	12	-	-	-	-	-	-	-	-	-	-	4	-	2,3,13	10												
	1	12	-	-	-	-	-	-	-	-	-	-	4	-	2,3,13	10												

* Prime Fan-Out.

† Ground inputs to gates not under test during ALL tests, unless otherwise noted.

1 The inputs to all gates must be ungrounded.

① Values @ 1000 pF load.

MTTLII

**INTEGRATED CIRCUITS
MC2100/MC2000 SERIES**

MTTL II

INTEGRATED CIRCUITS

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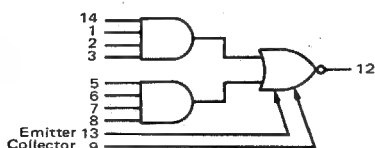
NUMERICAL INDEX
(Functions and Characteristics)

$V_{CC} = 5.0 \text{ Vdc}$, $T_A = 25^\circ\text{C}$

Function	Type		Output Loading Factor Each Output		Propagation Delay t _{pd} ns typ	Power Dissipation mW typ/pkg	Page No.
	Case 609, 93 0 to +75°C	Case 609 -55 to +125°C					
	MC2000 Series	MC2100 Series					
Expandable 2-Wide 4-Input AND-OR-INVERT Gate	MC2000 MC2050	MC2100 MC2150	9 5	11 6	7.0	27	4-66
Quad 2-Input NAND Gate	MC2001 MC2051	MC2101 MC2151	9 5	11 6	6.0	88	4-68
4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates	MC2002 MC2052	MC2102 MC2152	9 5	11 6	—	28	4-87
Dual 4-Input NAND Gate	MC2003 MC2053	MC2103 MC2153	9 5	11 6	6.0	44	4-64
Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate	MC2004 MC2054	MC2104 MC2154	9 5	11 6	7.0	36	4-70
Single 8-Input NAND Gate	MC2005 MC2055	MC2105 MC2155	9 5	11 6	8.0	22	4-62
Dual 4-Input Expander for AND-OR-INVERT Gates	MC2006 MC2056	MC2106 MC2156	9 5	11 6	—	14	4-85
Triple 3-Input NAND Gate	MC2007 MC2057	MC2107 MC2157	9 5	11 6	6.0	66	4-72
AND J-K Flip-Flop	MC2009 MC2059	MC2109 MC2159	9 5	11 6	f = 30 MHz	40	4-76
OR J-K Flip-Flop	MC2010 MC2060	MC2110 MC2160	9 5	11 6	f = 30 MHz	50	4-81
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC2013 MC2063	MC2113 MC2163	9 5	11 6	8.0	58	4-74

GATES

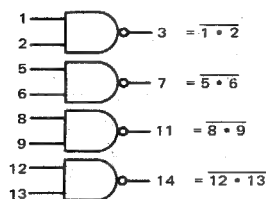
MC2000/MC2050
MC2100/MC2150
Expandable 2-Wide 4-Input
AND-OR-INVERT Gate



$$12 = (14 \cdot 1 \cdot 2 \cdot 3) + (5 \cdot 6 \cdot 7 \cdot 8) + \dots$$

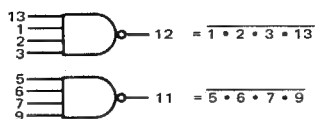
$t_{pd} = 7.0 \text{ ns typ}$
 $P_D = 27 \text{ mW typ/Pkg}$

MC2001/MC2051
MC2101/MC2151
Quad 2-Input NAND Gate



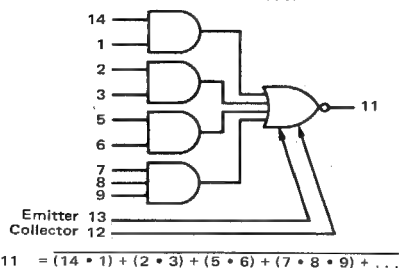
$t_{pd} = 6.0 \text{ ns typ}$
 $P_D = 88 \text{ mW typ/Pkg}$

MC2003/MC2053
MC2103/MC2153
Dual 4-Input NAND Gate



$t_{pd} = 6.0 \text{ ns typ}$
 $P_D = 44 \text{ mW typ/Pkg}$

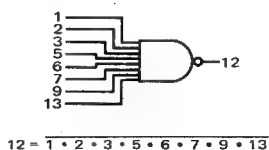
MC2004/MC2054
MC2104/MC2154
Expandable 4-Wide 2-2-2-3 Input
AND-OR-INVERT Gate



$$11 = (14 \cdot 1) + (2 \cdot 3) + (5 \cdot 6) + (7 \cdot 8 \cdot 9) + \dots$$

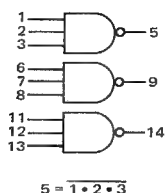
$t_{pd} = 7.0 \text{ ns typ}$
 $P_D = 36 \text{ mW typ/Pkg}$

MC2005/MC2055
MC2105/MC2155
Single 8-Input NAND Gate



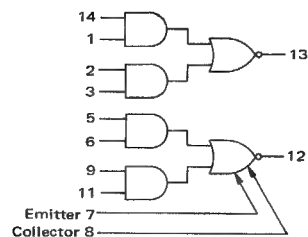
$t_{pd} = 8.0 \text{ ns typ}$
 $P_D = 22 \text{ mW typ/Pkg}$

MC2007/MC2057
MC2107/MC2157
Triple 3-Input NAND Gate



$t_{pd} = 6.0 \text{ ns typ}$
 $P_D = 66 \text{ mW typ/Pkg}$

MC2013/MC2063
MC2113/MC2163
Expandable Dual 2-Wide 2-Input
AND-OR-INVERT Gate

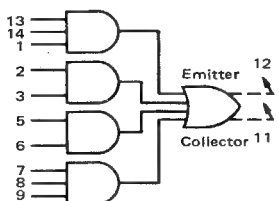


$t_{pd} = 8.0 \text{ ns typ}$ $P_D = 58 \text{ mW typ/Pkg}$

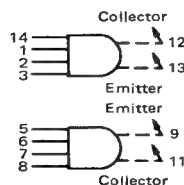
LOGIC DIAGRAMS (continued)

EXPANDERS

**MC2002/MC2052
MC2102/MC2152
4-Wide 3-2-2-3 Input Expander
For AND-OR-INVERT Gates**

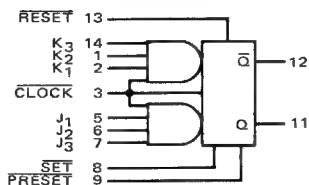
 $P_D = 28 \text{ mW typ/Pkg}$

**MC2006/MC2056
MC2106/MC2156
Dual 4-Input Expander For
AND-OR-INVERT Gates**

 $P_D = 14 \text{ mW typ/Pkg}$

- FLIP-FLOPS

MC2009/MC2059
MC2109/MC2159
AND J-K Flip-Flop

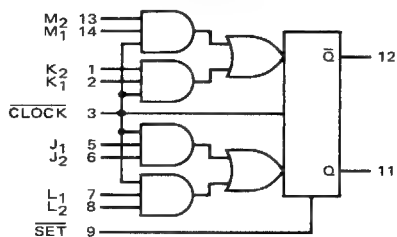


J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Where $J = J_1 \cdot J_2 \cdot J_3$
 $K = K_1 \cdot K_2 \cdot K_3$

$f = 30 \text{ MHz}$
 $P_D = 40 \text{ mW}$

MC2010/MC2060
MC2110/MC2160
OR J-K Flip-Flop



J	L	K	M	Q_n	Q_{n+1}
0	0	X	X	0	0
1	X	X	X	0	1
X	1	X	X	0	1
X	X	0	0	1	1
X	X	1	X	1	0
X	X	X	1	1	0

X = Don't Care

Where $J = J_1 \cdot J_2$
 $L = L_1 \cdot L_2$
 $K = K_1 \cdot K_2$
 $M = M_1 \cdot M_2$

$f = 30 \text{ MHz}$
 $P_D = 50 \text{ mW}$

MTTL II

GENERAL INFORMATION SECTION

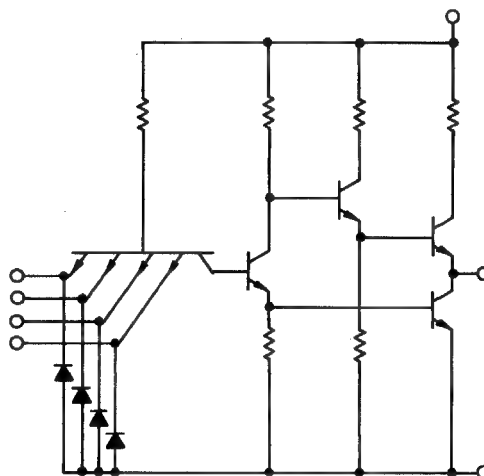
INTRODUCTION

MTTL II transistor-transistor logic is a high-speed, high-noise-immunity family of saturating integrated logic circuits.

The MTTL II family provides a speed extension of the medium-speed MTTL family. The circuits in the MTTL II family are identified by a multiple emitter input transistor and a two-stage active "pull-up" in the upper output network as shown in Figure 1.

The multiple emitter input configuration offers the maximum amount of logic capability in the minimum physical area and provides improved switching characteristics during turnoff. Clamp diodes are provided at each of the inputs to limit undershoot that occurs in typical system applications such as driving long interconnect wiring. The two-stage output configuration provides very low output impedances in each of the two output states. These low impedances result in excellent ac noise immunity and allow high-speed operation while driving large capacitive loads.

FIGURE 1 — TYPICAL MTTL II CIRCUIT



MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage — Continuous MC2100 Series MC2000 Series	+8.0 +7.0	V _{dc}
Supply Operating Voltage Range	4.5 to 6.0	V _{dc}
Input Voltage	+5.5	V _{dc}
Output Voltage	+5.5	V _{dc}
Operating Temperature Range MC2100 Series MC2000 Series	-55 to +125 0 to +75	°C
Storage Temperature Range Flat Package Plastic Package	-65 to +200 -55 to +125	°C
Maximum Junction Temperature MC2100 Series MC2000 Series	+175 +150	°C
Thermal Resistance - Junction To Case (θ_{JC}) Ceramic Flat Package Plastic Dual-In-Line	0.09 0.15	°C/mW
Thermal Resistance - Junction To Ambient (θ_{JA}) Ceramic Flat Package Plastic Dual-In-Line	0.26 0.30	°C/mW

TYPICAL CHARACTERISTICS

The following summary presents the typical operating characteristics of the MTTL II family. Unless otherwise indicated, the parameters are defined for $V_{CC} = +5.0$ volts and $T_A = +25^\circ\text{C}$.

Supply Voltage Operating Range = 4.5 to 6.0 volts

Operating Temperature Range:

MC2100/2150 Series = -55 to $+125^\circ\text{C}$

MC2000/2050 Series = 0 to $+75^\circ\text{C}$

Output Drive Capability

Other Gates (Output Loading Factor):

MC2100 Series = 11 MC2100 or MC2150 Series Gates.

MC2150 Series = 6 MC2100 or MC2150 Series Gates.

MC2000 Series = 9 MC2000 or MC2050 Series Gates.

MC2050 Series = 5 MC2000 or MC2050 Series Gates.

Capacitance = 600 pF

Output Impedance

High State = 10 ohms (unsaturated) nominal

Low State = 10 ohms nominal

Output Voltage Swing = 0.2 to 3.5 volts typical

Input Voltage Limits

+5.5 volts maximum

-0.5 volt minimum

Switching Threshold = 1.5 volts nominal

Input Impedance

High State = 400 k ohms nominal

Low State = 2.5 k ohms nominal

Worst-Case DC Noise Margin

High State - MC2100/2150 series 0.700 volt minimum

MC2000/2050 series 0.600 volt minimum

Low State - MC2100/2150 series 0.650 volt minimum

MC2000/2050 series 0.650 volt minimum

Power Dissipation

22 mW per gate typical

40-50 mW per flip-flop typical

Switching Speeds⁽¹⁾

Average Propagation Delay = 6.0 ns per gate typical

15 ns per flip-flop typical

Rise Time = 1.0 ns typical

Fall Time = 1.3 ns typical

Flip-Flop Clock Frequency (MC2109/MC2110 Series) = 30 MHz maximum

BREADBOARDING SUGGESTIONS

When breadboarding with any form of high-speed, high-performance TTL, the designer must continually be aware of the fact that he is working with the fastest form of saturating logic available in the industry today. The switching speeds, especially the frequencies associated with the very fast rise and fall times of the circuits, are in the RF range and good high-frequency layout techniques should be used. The following breadboarding suggestions have been included to help the designer in his initial circuit layout. In many cases the breadboarding suggestions will have to be modified to meet the requirements of the designer's specific application.

Power and Ground Distribution

Special care should be taken to insure adequate distribution of power and ground systems. The typical rate of change of currents and voltages for a single MTTL II gate is in the range of 10^7 A/s and 10^8 V/s respectively. These figures reflect the necessity for a low-impedance power supply and ground distribution system, if transients are to be minimized and noise margins maintained. The use of AWG No. 20 wire or larger is often required. For printed circuitry, line widths of 100 mils or more are often necessary. A ground plane is desirable when using a large number of units.

Bypassing

To reduce supply transients, the breadboard should be bypassed at the point where power is supplied to the board and at intervals throughout the board. The use of a single bypass capacitor at the output terminal of the power supply is not adequate in a breadboard utilizing the fast rise and fall time MTTL II circuits. A comparatively large, low-inductance type capacitor (in the $1.0\ \mu\text{F}$ range) is suggested at the point where power and ground enter the board. In many cases it has been found that distributing $0.01\ \mu\text{F}$ capacitors for every five packages throughout a breadboard is adequate to suppress normal switching transients. It is also suggested that a bypass capacitor be placed in close proximity to any circuit driving a large capacitive load.

Power Dissipation

The standard supply voltage of the MTTL II logic circuits is +5.0 Vdc. The typical average dc power dissipation is given for each MTTL II circuit.⁽²⁾ It should be noted that the totem pole output common to all high level MTTL circuits has an associated ac power dissipation factor. This factor results from the timing overlap of the upper and lower output transistors during the normal switching operation and is typically 0.7 mW/MHz/output for a 15 pF load. This ac power dissipation should be added when calculating the total power requirements of the MTTL II circuits.

Unused Inputs and Unused Gates

The unused inputs of any MTTL II logic circuit should not be left open, and can either be tied to the used inputs or returned to the supply voltage. This will reduce any potential problems resulting from external noise. If the inputs are returned to the supply voltage, care should be taken to insure that the supply voltage does not exceed the maximum rated input voltage of 5.5 volts. If the supply can exceed 5.5 volts, the unused inputs must be returned to a lower voltage. The total number of inputs that can be tied to the output of any driving gate is 50. (This is defined as high state output loading factor.) It should be noted that the low state output loading rules must still be maintained. The minimum logical "1" level for the high state output loading is summarized for $V_{CC} = 5.0\ \text{V}$, $V_{IL} = 0.45\ \text{V}$ and $I_{OH} = -5.0\ \text{mA}$:

MC2100/2150 Series - $V_{OH} = 2.7$ volts minimum @ -55°C

MC2000/2050 Series - $V_{OH} = 2.9$ volts minimum @ 0°C

The unused inputs of the various flip-flops may be tied back to their associated outputs. To determine which outputs are related to each set of inputs by internal feedback, refer to the circuit schematics.

The inputs of any unused gate in a package should be grounded. This places the gate in its lowest power condition and will help to eliminate unnecessary power drain.

Expanders and Expander Nodes

The ORing nodes of all the MTTL II AND-OR-INVERT gates are made available for expanding the number of AND gates to 10. Since these are comparatively high-impedance nodes, care should be taken to minimize capacitive loading on the expander terminals if switching speed is to be maintained. When an expander is to be used with an expandable AND-OR-INVERT gate, it should be placed as close as possible to the gate being expanded. The increase in the average propagation delay per AND gate added to an expandable AND-OR-INVERT gate is typically 1.0 ns/AND gate. The increase in average propagation delay as a function of capacitance added to the expander nodes is typically 0.7 ns/pF.

Output OR (AND) Function

Unlike the MTTL family of logic circuits, the outputs of the MTTL II logic circuits cannot be tied together to perform the output OR, or more correctly, the output AND function. If the outputs of the MTTL II family devices are tied together, it would be possible for the lower output transistor of one circuit and the upper output transistor of another circuit to be "on" simultaneously. This condition provides a low-impedance path from V_{CC} to ground and the current that flows (approximately I_{SC}) exceeds the guaranteed sink current. As a result, the saturated state cannot be maintained and the desired logic function is not satisfied.

Operating Characteristics of Flip-Flops

The general operating characteristics and restrictions for the MC2109/MC2110 series J-K flip-flops are as follows:

The clocked inputs are inhibited when the clock is in the low state, and data should be applied and allowed to settle. The clocked inputs are enabled when the clock goes high and data enters the flip-flop. The data is temporarily stored in the charge-storage section (temporary memory) while the clock is in the high state. This data is transferred to the bistable section on the negative clock transition.

The data on the clocked inputs should not be changed while the clock is in the high state. Data changes during this clock condition require 300 ns settling time.

The direct SET, PRESET, and RESET inputs do not directly affect the charge-storage section and therefore should not be used while the clock is high. On the negative transition of the clock, previously stored data may override the asynchronous set output state. Further, the direct SET, PRESET, and RESET inputs do not

MTTL II

GENERAL INFORMATION SECTION

override the clock and will not control the state of the flip-flop until 100 ns after the negative transition of the clock. The clock signal must conform to the following boundary conditions at +125°C.

Maximum guaranteed clock frequency	= 30 MHz
Maximum clock fall time	= 100 ns
Minimum clock pulse width	= 15 ns
Minimum clock pulse amplitude	= 1.8 V
Maximum negative clock voltage	= -0.5 V

Note: These boundary conditions for operation are not defined as occurring simultaneously.

The transfer of data from the charge storage section to the bistable section is essentially an ac operation and thus results in the restriction of the clock fall time. If the clock fall time is greater than 100 ns, the information retained in the charge-storage section may not be transferred to the bistable section. The flip-flop will operate from very low frequencies to 30 MHz as long as the clock fall time is less than or equal to 100 ns.

Large negative clock excursions may cause incorrect data transfers to the bistable section during the transfer cycles. Therefore, the most negative clock signal should be limited to -0.5 volt.

(1) The switching characteristics of the MTTL II family are defined with respect to the associated transitions of the voltage waveforms. The average propagation delay is defined as the average of the turn-on delay and the turn-off delay measured from the 1.5 V point of the input to the 1.5 V point of the associated output transition or:

$$t_{pd} = \frac{t_{on} + t_{off}}{2} \text{ ns.}$$

Rise time is defined as the positive going transition of the output from the 1.0 V to the 2.0 V level. Fall time is defined as the negative transition of the output from the 2.0 V to the 1.0 V level.

(2)

$$P_D = \frac{I_{PDL} + I_{PDH}}{2} (V_{CC})$$

where I_{PDL} and I_{PDH} are the typical dc current drains at $V_{CC} = +5.0$ V.

MC2000/2050 and 2100/2150 MTTL II* series integrated circuits are electrically interchangeable with SUHL II† series logic circuits as shown in the cross reference below.

SG SF NUMBER	Description	-55 to +125°C		0 to +75°C	
		Fan-Out = 11	Fan-Out = 6	Fan-Out = 9	Fan-Out = 5
SG210-213	Expandable 2-Wide 4-Input AND-OR-INVERT Gate	MC2100	MC2150	MC2000	MC2050
SG220-223	Quad 2-Input NAND Gate	MC2101	MC2151	MC2001	MC2051
SG230-233	4-Wide 3-2-2-3 Input Expander For AND-OR-INVERT Gates	MC2102	MC2152	MC2002	MC2052
SG240-243	Dual 4-Input NAND Gate	MC2103	MC2153	MC2003	MC2053
SG250-253	Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate	MC2104	MC2154	MC2004	MC2054
SG260-263	Single 8-Input NAND Gate	MC2105	MC2155	MC2005	MC2055
SG270-273	Dual 4-Input Expander For AND-OR-INVERT Gates	MC2106	MC2156	MC2006	MC2056
-	Triple 3-Input NAND Gate	MC2107	MC2157	MC2007	MC2057
SF250-253	AND J-K Flip-Flop	MC2109	MC2159	MC2009	MC2059
SF260-263	OR J-K Flip-Flop	MC2110	MC2160	MC2010	MC2060
SG310-313	Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC2113	MC2163	MC2013	MC2063

*Trademark of Motorola Inc.

†Trademark of Sylvania Electric Products, Inc.

GENERAL INFORMATION

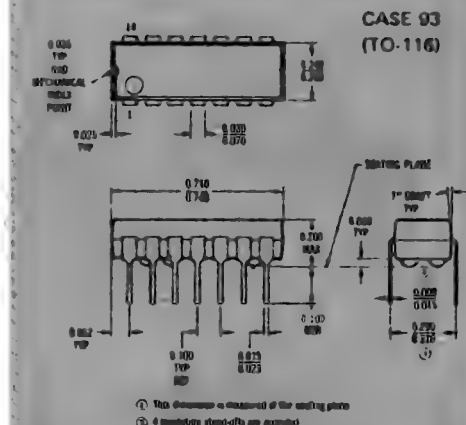
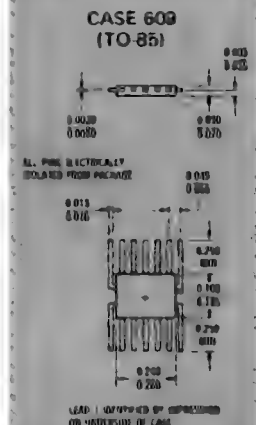
DEFINITIONS

V_{Vin} "0"	Input breakdown voltage (ON level)
V_{Vin} "1"	Input breakdown voltage (OFF level)
f_{Tog}	Toggle frequency
I_C	Collector current
I_F	Input forward current
I_{FC}	Forward current of clock input
I_{in}	Input current
$2 I_{in}$	2-times the Input Current
$4 I_{in}$	4-times the Input Current
I_L	Inverse bias current
I_{LC}	Inverse bias current of the clock input
I_{max}	Maximum rated power supply current with V_{max} applied
I_O	Output breakdown current
I_{OH}	Output high current
I_{OL}	Output low current
I_{OLK}	Output leakage current
I_{PDH}	Power supply drain with inputs high
I_{PDL}	Power supply drain with inputs low
I_R	Input reverse current with V_{in} applied
I_{RC}	Reverse current of clock input
I_{SC}	Short circuit current obtained from device output when one or more inputs are low
I_V	Prime Fan-Out
PRF	Pulse repetition frequency
PW	Pulse width
Sid	Standard fan-out
t_f	Fall time
t_{off}	Turn-off delay time

t_{on}	Turn-on delay time
t_{Preset}	The minimal time necessary before the \overline{SET} , \overline{PRESET} , or \overline{RESET} inputs can control the flip-flop after the negative clock edge
t_r	Rise time
Δt_{pd}	Average increase in propagation delay per AND gate of expander when connected to an AND-OR INVERT gate.
$\Delta t_{pd}/PF$	Increased propagation delay caused by additional capacitance at expansion points.
TP_{in}	Test point at input of device under test
TP_{out}	Test point at output of device under test
V_{amp}	Voltage amplitude
V_{CC}	Power supply voltage
V_{CCH}	High power supply voltage
V_{CE}	Collector-emitter voltage
V_{CR}	Collector voltage obtained thru 1.3 k ohm resistor from V_{CC} .
V_{CRH}	Collector voltage obtained thru 1.3 k ohm resistor from V_{CCH} .
V_{E1}, V_{E2}	Emitter voltage
V_{E3}	
V_{EN}	Enable voltage level
V_{IH}	Voltage for high input voltage state
V_{IHx}	Reduced supply voltage to hold input above three-hold and to prevent noise from entering the device
V_{IL}	Voltage for low input voltage state
V_{INH}	Inhibit voltage level
V_{max}	Maximum rated power supply voltage (V_{CC})
V_{OH}	Output high voltage with I_{OH} flowing out of pin
V_{OL}	Output low voltage with I_{OL} flowing into pin
$V_{out} "0"$	Output low voltage with $V_{th} "1"$ applied
$V_{out} "1"$	Output high voltage with $V_{th} "0"$ applied
V_R	Input reverse voltage
$V_{th} "0"$	Input logic "0" threshold voltage
$V_{th} "1"$	Input logic "1" threshold voltage

PACKAGING

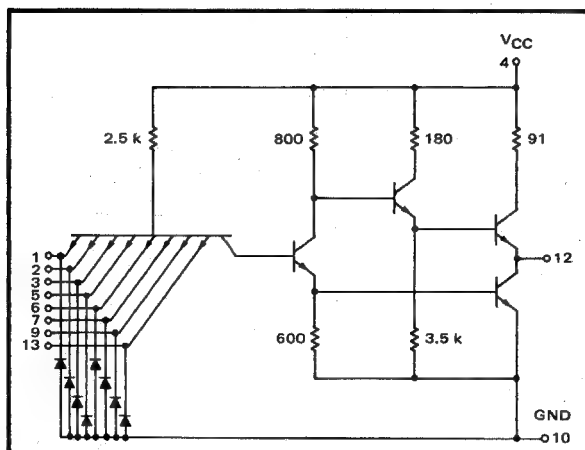
All MTTL II integrated circuits are available in the TO-25 14-lead flat package. MC2000 series is also available in the 14-lead dual in-line plastic package. To order the flat package, add suffix "F" to the basic type number; to order plastic packages, add suffix "P".



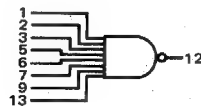
SINGLE 8-INPUT "NAND" GATE

MTTL II MC2100/2000 series

MC2105 • MC2155 MC2005 • MC2055



This device is an 8-input NAND gate. It is useful when processing a large number of variables, such as in encoders or decoders.



Positive Logic:

$$12 = \overline{1 \cdot 2 \cdot 3 \cdot 5 \cdot 6 \cdot 7 \cdot 9 \cdot 13}$$

Negative Logic:

$$12 = \overline{1 + 2 + 3 + 5 + 6 + 7 + 9 + 13}$$

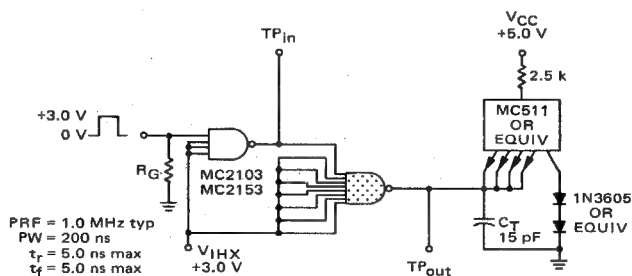
Total Power Dissipation = 22 mW typ/Pkg

Propagation Delay Time = 8.0 ns typ

SERIES	INPUT LOADING FACTOR (I _F)	OUTPUT DRIVE (I _{OL})	TEMPERATURE RANGE
MC2105 MC2155	1 -2.0 mA	11 MC2100 series Gates 22 mA 6 MC2100 series Gates 12 mA	-55°C to +125°C
MC2005 MC2055	1 -2.5 mA	9 MC2000 series Gates 22.5 mA 5 MC2000 series Gates 12.5 mA	0°C to +75°C

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



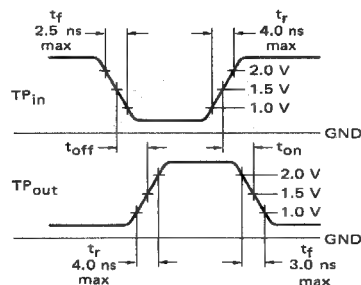
NOTES:

R_G = 50 ohms

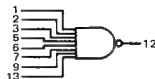
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.

Scope rise time < 1.0 ns

Probe capacitance < 5.0 pF



Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.



@ Test
Temperatur

MC2105*, MC2155	$\left\{ \begin{array}{l} -55^{\circ}\text{C} \\ +25^{\circ}\text{C} \\ +125^{\circ}\text{C} \end{array} \right.$
MC2005*, MC2055	$\left\{ \begin{array}{l} 0^{\circ}\text{C} \\ +25^{\circ}\text{C} \\ +75^{\circ}\text{C} \end{array} \right.$

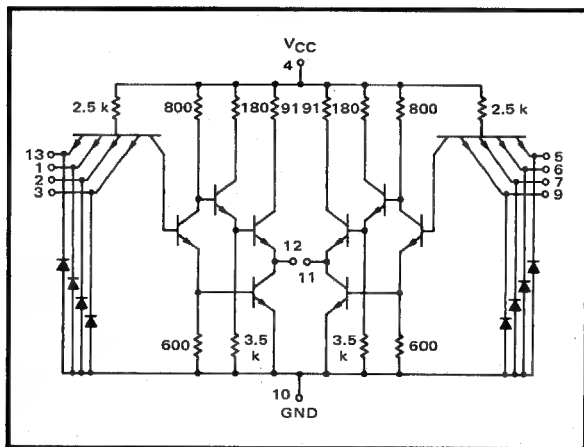
TEST CONDITIONS													
mA					Volts								
I _{OL}		I _{OH}		I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}
Pr*	Std	Pr*	Std										
22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-
22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-
22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:													
I _{OL}	I _{OH}	I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}	Gnd	
-	-	-	-	-	2,3,5,6 7,9,13	-	-	-	4	-	-	1, 10	
-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7, 9,10,13	
-	-	-	-	-	1	-	1	-	4	-	-	10	
-	-	1	-	-	-	-	-	-	4	-	-	10	
-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7, 9,10,13	
12	-	-	-	-	-	1	-	-	4	-	-	10-	
-	12	-	-	-	-	-	1	-	4	-	-	10-	
-	-	-	-	-	-	-	-	12	4	-	-	1,2,3,5,6, 9,10,13	
-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 9,10,12,13	
12	-	-	-	1	-	-	-	-	4	-	-	10	
-	12	-	1	-	-	-	-	-	4	-	-	10	
-	-	-	-	-	-	-	-	-	-	4	-	1, 10	
-	-	-	-	-	-	-	-	-	4	-	-	10	
-	-	-	-	-	-	-	-	-	4	-	-	1, 10	
Pulse In	Pulse Out												
1	12	-	-	-	-	-	-	-	4	-	-	2,3,5,6, 7,9,13	10
1	12	-	-	-	-	-	-	-	4	-	-	2,3,5,6, 7,9,13	10
1	12	-	-	-	-	-	-	-	4	-	-	2,3,5,6, 7,9,13	10
1	12	-	-	-	-	-	-	-	4	-	-	2,3,5,6, 7,9,13	10

* Prime Fan-Out.

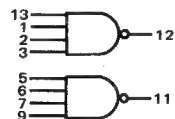
DUAL 4-INPUT "NAND" GATE

MTTL II MC2100/2000 series

MC2103 • MC2153 MC2003 • MC2053



This device consists of two 4-input NAND gates. The gates can be cross coupled to form a multiple-input R-S flip-flop or a circuit for eliminating contact bounce.



Positive Logic:

$$12 = 1 \cdot 2 \cdot 3 \cdot 13$$

Negative Logic:

$$12 = 1 + 2 + 3 + 13$$

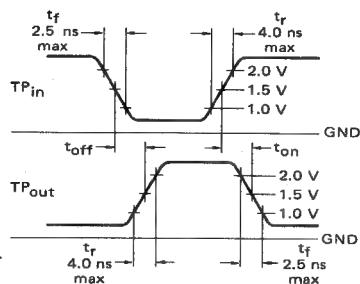
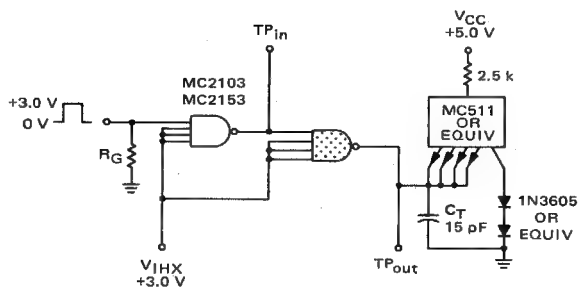
Total Power Dissipation = 44 mW typ/Pkg

Propagation Delay Time = 6.0 ns typ

SERIES	INPUT LOADING FACTOR (I_F)	OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
MC2103 MC2153	1 -2.0 mA	11 6 MC2100 series Gates 22 mA 6 MC2100 series Gates 12 mA	-55°C to +125°C
MC2003 MC2053	1 -2.5 mA	9 MC2000 series Gates 22.5 mA 5 MC2000 series Gates 12.5 mA	0°C to +75°C

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



NOTES:

$R_G = 50$ ohms

C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.

Scope rise time < 1.0 ns

Probe capacitance < 5.0 pF

Ground inputs to all gates not under test.

PRF = 1.0 MHz typ

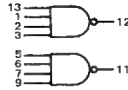
PW = 200 ns

$t_r = 5.0$ ns max

$t_f = 5.0$ ns max

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in a similar manner. Further, test procedures are shown for only one input of the gate being tested. To complete testing, sequence through remaining inputs.



MC2103*, MC2153

MC2003*, MC2053

@ Test
Temperature

-55°C
+25°C
+125°C
0°C
+25°C
+75°C

TEST CONDITIONS															Unit
mA					Volts										
I _{OL}		I _{OH}		I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}		
Pr*	Std	Pr*	Std												
dc	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-	
dc	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0	
dc	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-	
dc	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-	
dc	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0	
dc	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-	
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:															
dc	I _{OL}	I _{OH}	I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}	Gnd†		
dc	-	-	-	-	-	2, 3, 13	-	-	-	4	-	-	1, 10		
dc	-	-	-	-	-	1	-	-	-	4	-	-	2, 3, 10, 13		
dc	-	-	-	-	-	1	-	-	-	4	-	-	10		
dc	-	-	1	-	-	-	-	-	-	4	-	-	10		
dc	-	-	1	-	-	-	-	-	-	4	-	-	2, 3, 10, 13		
dc	12	-	-	-	-	-	1	-	-	4	-	-	10		
dc	-	12	-	-	-	-	-	1	-	4	-	-	10		
dc	-	-	-	-	-	-	-	-	12	4	-	-	1, 2, 3, 10, 13		
dc	-	-	-	-	-	-	-	-	-	4	-	-	1, 2, 3, 10, 12, 13		
dc	12	-	-	-	1	-	-	-	-	4	-	-	10		
dc	-	12	-	1	-	-	-	-	-	4	-	-	10		
dc	-	-	-	-	-	-	-	-	-	-	4	-	1, 5, 10		
dc	-	-	-	-	-	-	-	-	-	4	-	-	10†		
dc	-	-	-	-	-	-	-	-	-	4	-	-	1, 5, 10		
ns	Pulse In		Pulse Out		-	-	-	-	-	-	4	-	2, 3, 13	10	
ns	1	12	-	-	-	-	-	-	-	4	-	-	2, 3, 13	10	
ns	1	12	-	-	-	-	-	-	-	4	-	-	2, 3, 13	10	
ns	1	12	-	-	-	-	-	-	-	4	-	-	2, 3, 13	10	

* Prime Fan-Out.

† Ground inputs to gate not under test during ALL tests unless otherwise noted.

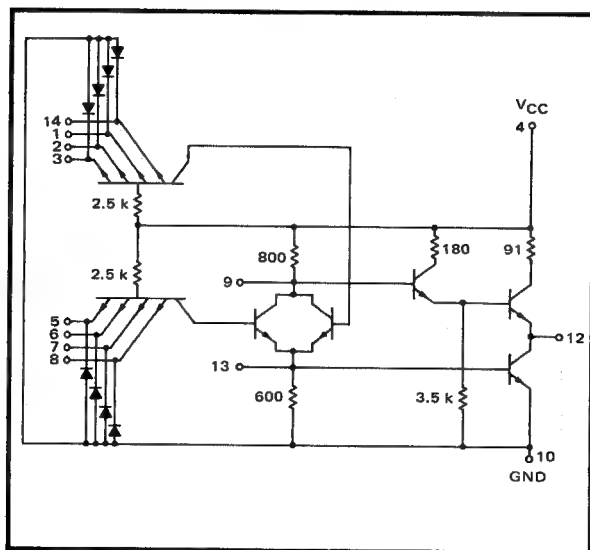
‡ The inputs of both gates must be ungrounded.

MC2103, MC2153/MC2003, MC2053 (continued)

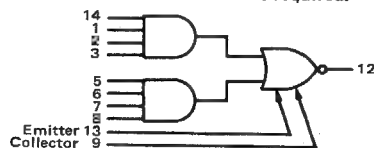
EXPANDABLE 2-WIDE 4-INPUT "AND-OR-INVERT" GATE

MTTL II MC2100/2000 series

MC2100 • MC2150 MC2000 • MC2050



This device consists of two 4-input AND gates ORed together and driving an output inverter. The ORing nodes are available for expansion, and up to 10 AND gates can be ORed together using the MC2102 or the MC2106 series expanders. Since switching speed is affected by the amount of capacitance on the expander nodes, care should be taken to minimize this capacitance to maintain switching speeds. This gate is usable for construction of half adders and other applications where the exclusive OR function is required.



Positive Logic:

$$12 = (\overline{1 \cdot 2 \cdot 3 \cdot 14}) + (\overline{5 \cdot 6 \cdot 7 \cdot 8}) + (\text{Expanders})$$

Negative Logic:

$$12 = (\overline{1 + 2 + 3 + 14}) \cdot (\overline{5 + 6 + 7 + 8}) \cdot (\text{Expanders})$$

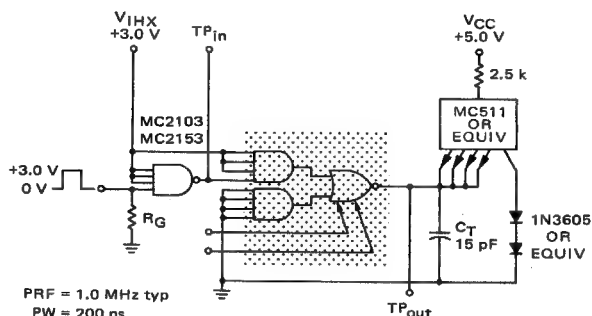
Total Power Dissipation = 27 mW typ/Pkg

Propagation Delay Time = 7.0 ns typ

SERIES	INPUT LOADING FACTOR (I _F)	OUTPUT DRIVE (I _{OL})	TEMPERATURE RANGE
MC2100 MC2150	1 -2.0 mA	11 MC2100 series Gates 22 mA 6 MC2100 series Gates 12 mA	-55°C to +125°C
MC2000 MC2050	1 -2.5 mA	9 MC2000 series Gates 22.5 mA 5 MC2000 series Gates 12.5 mA	0°C to +75°C

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



PRF = 1.0 MHz typ
PW = 200 ns
 $t_r = 5.0$ ns max
 $t_f = 5.0$ ns max

NOTES:

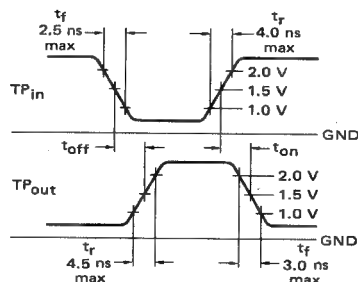
$R_G = 50$ ohms

C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.

Scope rise time < 1.0 ns

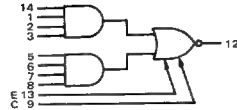
Probe capacitance < 5.0 pF

Expander pins should be left open when measuring switching times.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.



@ Test Temperature
 MC2100*, MC2150
 MC2000*, MC2050

TEST CONDITIONS															Gnd
mA				Volts											
I _{OL}		I _{OH}		I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}		
Pr*	Std	Pr*	Std												
C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-	
C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0	
C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-	
C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-	
C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0	
C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-	
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:															
I _{OL}	I _{OH}	I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}				
dc	-	-	-	-	-	2,3,14	-	-	-	4	-	-	1, 5, 6, 7, 8, 10		
dc	-	-	-	-	-	1	-	-	-	4	-	-	2, 3, 5, 6, 7, 8, 10, 14		
dc	-	-	-	-	-	1	-	-	-	4	-	-	5, 6, 7, 8, 10		
dc	-	-	1	-	-	-	-	-	-	4	-	-	5, 6, 7, 8, 10		
dc	-	-	1	-	-	-	-	-	-	4	-	-	2, 3, 5, 6, 7, 8, 10, 14,		
dc	12	-	-	-	-	-	1	-	-	4	-	-	5, 6, 7, 8, 10		
dc	-	12	-	-	-	-	-	1	-	4	-	-	5, 6, 7, 8, 10		
dc	-	-	-	-	-	-	-	-	12	4	-	-	1, 2, 3, 5, 6, 7, 8, 10, 14		
dc	-	-	-	-	-	-	-	-	-	4	-	-	1, 2, 3, 5, 6, 7, 8, 10, 12, 14		
dc	12	-	-	-	1	-	-	-	-	4	-	-	5, 6, 7, 8, 10		
dc	-	12	-	1	-	-	-	-	-	4	-	-	5, 6, 7, 8, 10		
dc	-	-	-	-	-	-	-	-	-	-	4	-	1, 2, 3, 5, 6, 7, 8, 10, 14		
dc	-	-	-	-	-	-	-	-	-	4	-	-	10		
dc	-	-	-	-	-	-	-	-	-	4	-	-	1, 2, 3, 5, 6, 7, 8, 10, 14		
Pulse In		Pulse Out		-	-	-	-	-	-	4	-	-	2,3,14	5, 6, 7, 8, 10	
1		12		-	-	-	-	-	-	4	-	-	2,3,14	5, 6, 7, 8, 10	
1		12		-	-	-	-	-	-	4	-	-	2,3,14	5, 6, 7, 8, 10	
1		12		-	-	-	-	-	-	4	-	-	2,3,14	5, 6, 7, 8, 10	

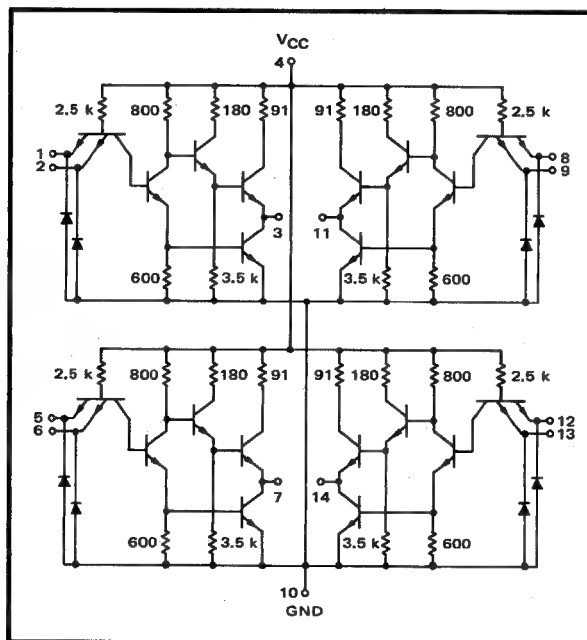
*Prime Fan-Out.

MC2100, MC2150/MC2000, MC2050 (continued)

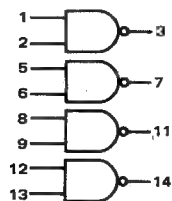
QUAD 2-INPUT "NAND" GATE

MTTL II MC2100/2000 series

MC2101 • MC2151 MC2001 • MC2051



This device consists of four 2-input NAND gates. The four gates in a single package represent increased functional flexibility. For example, a dual set-reset flip-flop may be obtained if each pair of gates is externally cross-coupled.



Positive Logic:

$$3 = 1 \cdot 2$$

Negative Logic:

$$3 = 1 + 2$$

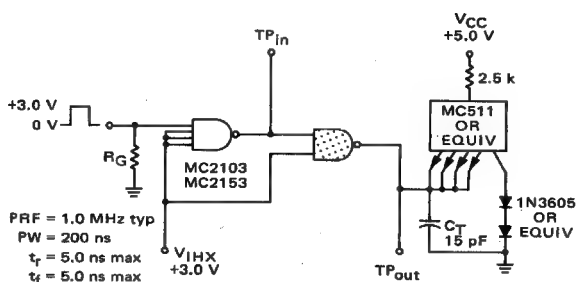
Total Power Dissipation = 88 mW typ/Pkg

Propagation Delay Time = 6.0 ns typ

SERIES	INPUT LOADING FACTOR (I _F)	OUTPUT DRIVE (I _{OL})	TEMPERATURE RANGE
MC2101 MC2151	1 -2.0 mA	11 MC2100 series Gates 22 mA 6 MC2100 series Gates 12 mA	-55°C to +125°C
MC2001 MC2051	1 -2.5 mA	9 MC2000 series Gates 22.5 mA 5 MC2000 series Gates 12.5 mA	0°C to +75°C

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



NOTES:

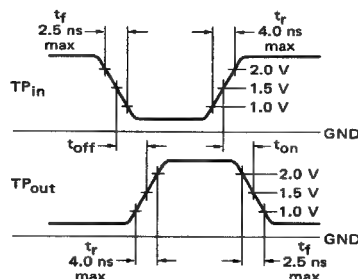
R_G = 50 ohms

C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.

Scope rise time < 1.0 ns

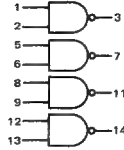
Probe capacitance < 5.0 pF

Ground inputs to all gates not under test.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in a similar manner. Further, test procedures are shown for only one input of the gate being tested. The other input is tested in the same manner.



@ Test Temperature
 MC2101*, MC2151 {
 -55°C
 +25°C
 +125°C
 MC2001*, MC2051 {
 0°C
 +25°C
 +75°C

TEST CONDITIONS														
mA					Volts									
I _{OL}		I _{OH}		I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}	
Pr*	Std	Pr*	Std											
22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-	
22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0	
22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-	
22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-	
22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0	
22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-	
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:														
I _{OL}	I _{OH}	I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}	Gnd†		
-	-	-	-	-	2	-	-	-	4	-	-	1, 10		
-	-	-	-	-	1	-	-	-	4	-	-	2, 10		
-	-	-	-	-	1	-	-	-	4	-	-	10		
-	-	1	-	-	-	-	-	-	4	-	-	10		
-	-	1	-	-	-	-	-	-	4	-	-	2, 10		
3	-	-	-	-	-	1	-	-	4	-	-	10		
-	3	-	-	-	-	-	1	-	4	-	-	10		
-	-	-	-	-	-	-	-	3	4	-	-	1, 2, 10		
-	-	-	-	-	-	-	-	-	4	-	-	1, 2, 3, 10		
3	-	-	-	1	-	-	-	-	4	-	-	10		
-	3	-	1	-	-	-	-	-	4	-	-	10		
-	-	-	-	-	-	-	-	-	-	4	-	1, 5, 8, 10, 12		
-	-	-	-	-	-	-	-	-	4	-	-	10†		
-	-	-	-	-	-	-	-	-	4	-	-	1, 5, 8, 10, 12		
Pulse In	Pulse Out													
1	3	-	-	-	-	-	-	-	4	-	2	10		
1	3	-	-	-	-	-	-	-	4	-	2	10		
1	3	-	-	-	-	-	-	-	4	-	2	10		
1	3	-	-	-	-	-	-	-	4	-	2	10		

Characteristic	Symbol	Pin Under Test	MC2101, MC2151 Test Limits						MC2001, MC2051 Test Limits						Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:													Gnd†
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C			I _{OL}	I _{OH}	I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max															
Input																													
Forward Current	I _F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	2	-	-	-	4	-	-	1, 10	
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2, 10	
Inverse Beta Current	I _L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	10	
Breakdown Voltage	BV _{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	4	-	-	10		
	BV _{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	4	-	-	2, 10		
Output																													
Output Voltage	V _{out} "0"	3	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	3	-	-	-	-	-	1	-	-	4	-	-	10	
	V _{out} "1"	3	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	Vdc	-	3	-	-	-	-	1	-	4	-	-	10		
Leakage Current	I _{OLK}	3	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	3	4	-	-	1, 2, 10	
Short-Circuit Current	I _{SC}	3	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1, 2, 3, 10	
Output Voltage	V _{OL}	3	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	3	-	-	-	1	-	-	-	-	4	-	-	10	
	V _{OH}	3	2.70	-	3.10	-	3.15	-	2.9	-	3.0	-	3.0	-	Vdc	-	3	-	1	-	-	-	-	-	4	-	-	10	
Power Requirements (Total Device)																													
Maximum Power Supply Current	I _{max}	4	-	-	-	26	-	-	-	-	-	-	27	-	-	mAdc	-	-	-	-	-	-	-	-	-	4	-	1, 5, 8, 10, 12	
Power Supply Drain	I _{PDH}	4	-	30	-	30	-	30	-	40	-	40	-	40	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10‡	
	I _{PDL}	4	-	15	-	15	-	15	-	20	-	20	-	20	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1, 5, 8, 10, 12	
Switching Parameters																													
Turn-On Delay	t _{on}	1, 3	-	-	-	10	-	-	-	-	-	-	10	-	-	ns	Pulse In	Pulse Out	-	-	-	-	-	-	4	-	2	10	
Turn-Off Delay	t _{off}	1, 3	-	-	-	10	-	-	-	-	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	4	-	2	10	
Rise Time	t _r	1, 3	-	-	-	4.0	-	-	-	-	-	-	4.0	-	-	ns	1	3	-	-	-	-	-	-	4	-	2	10	
Fall Time	t _f	1, 3	-	-	-	2.5	-	-	-	-	-	-	2.5	-	-	ns	1	3	-	-	-	-	-	-	4	-	2	10	

*Prime Fan-Out

†Ground inputs to gates not under test during ALL tests unless otherwise noted.

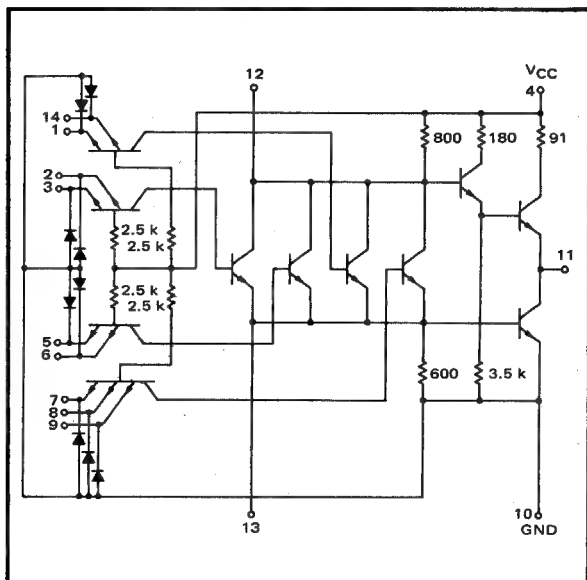
‡The inputs of all gates must be ungrounded.

MC2101, MC2151/MC2001, MC2051 (continued)

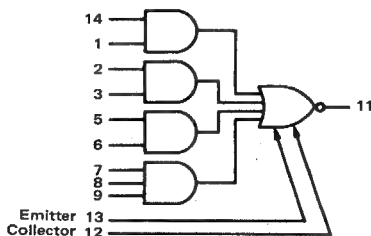
**EXPANDABLE
4-WIDE 2-2-2-3 INPUT
"AND-OR-INVERT" GATE**

MTTL II MC2100/2000 series

**MC2104 • MC2154
MC2004 • MC2054**



This device consists of three 2-input and one 3-input AND gates ORed together and driving an output inverter. The ORing nodes are made available for expansion, and up to 10 AND gates can be ORed together using the MC2102 or the MC2106 series expanders. Since switching speed is affected by the amount of capacitance on the expander nodes, care should be taken to minimize this capacitance to maintain switching speeds.



Positive Logic:

$$11 = (14 \cdot 1) + (2 \cdot 3) + (5 \cdot 6) + (7 \cdot 8 \cdot 9) + (\text{Expanders})$$

Negative Logic:

$$11 = (14 + 1) \cdot (2 + 3) \cdot (5 + 6) \cdot (7 + 8 + 9) \cdot (\text{Expanders})$$

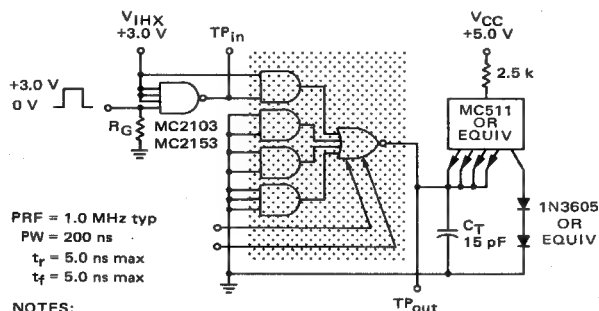
Total Power Dissipation = 36 mW typ/Pkg

Propagation Delay Time = 7.0 ns typ

SERIES	INPUT LOADING FACTOR (I _F)	OUTPUT DRIVE (I _{OL})	TEMPERATURE RANGE
MC2104 MC2154	1 -2.0 mA	11 MC2100 series Gates 22 mA 6 MC2100 series Gates 12 mA	-55°C to +125°C
MC2004 MC2054	1 -2.5 mA	9 MC2000 series Gates 22.5 mA 5 MC2000 series Gates 12.5 mA	0°C to +75°C

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



PRF = 1.0 MHz typ
PW = 200 ns
tr = 5.0 ns max
tf = 5.0 ns max

NOTES:

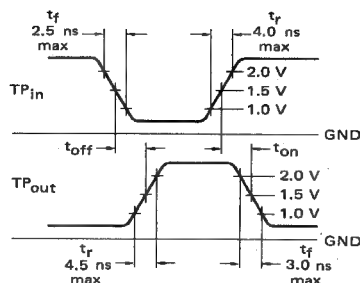
RG = 50 ohms

CT = the total parasitic capacitance which includes probe, wiring, and load capacitances.

Scope rise time < 1.0 ns

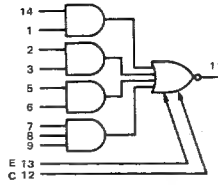
Probe capacitance < 5.0 pF

Expander pins should be left open when measuring switching times.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.



MC2104*, MC2154

MC2004*, MC2054

@ Test
Temperature

-55°C

+25°C

+125°C

0°C

+25°C

+75°C

TEST CONDITIONS

mA

Volts

	I_{OL}		I_{OH}		I_{in}	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{CC}	V_{CCH}	V_{IHx}
	Pr*	Std	Pr*	Std										
-55°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-
+25°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
+125°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-
0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
+25°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
+75°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-

TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:

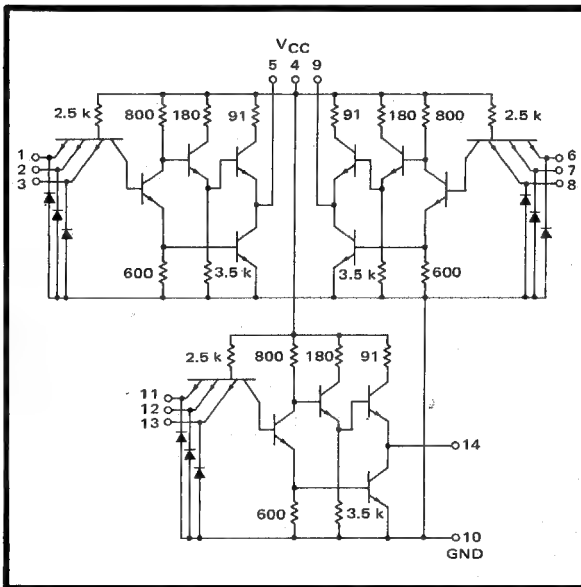
Characteristic	Symbol	Pin Under Test	MC2104, MC2154 Test Limits						MC2004, MC2054 Test Limits						Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:														Gnd
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C			I _{OL}	I _{OH}	I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max																
Input																														
Forward Current	I _F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	14	-	-	-	4	-	-	-	1,2,3,5,6,7,8,9,10	
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	-	2,3,5,6,7,8,9,10,14	
Inverse Beta Current	I _L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	-	2,3,5,6,7,8,9,10	
Breakdown Voltage	BV _{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	-	2,3,5,6,7,8,9,10	
	BV _{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	-	2,3,5,6,7,8,9,10,14	
Output																														
Output Voltage	V _{out} "0"	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11	-	-	-	-	-	1	-	-	4	-	-	-	2,3,5,6,7,8,9,10	
	V _{out} "1"	11	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	Vdc	-	11	-	-	-	-	-	1	-	4	-	-	-	2,3,5,6,7,8,9,10	
Leakage Current	I _{OLK}	11	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	11	4	-	-	-	1,2,3,5,6,7,8,9,10,14	
Short-Circuit Current	I _{SC}	11	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	-	1,2,3,5,6,7,8,9,10,11,14	
Output Voltage	V _{OL}	11	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	11	-	-	-	1	-	-	-	-	4	-	-	-	2,3,5,6,7,8,9,10	
	V _{OH}	11	2.70	-	3.10	-	3.15	-	2.9	-	3.0	-	3.0	-	Vdc	-	11	-	1	-	-	-	-	-	4	-	-	-	2,3,5,6,7,8,9,10	
Power Requirements (Total Device)																														
Maximum Power Supply Current	I _{max}	4	-	-	-	17	-	-	-	-	-	18	-	-	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	-	1,2,3,5,6,7,8,9,10,14	
Power Supply Drain	I _{PDH}	4	-	12	-	12	-	12	-	16	-	16	-	16	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	-	10	
	I _{PDL}	4	-	10	-	10	-	10	-	13	-	13	-	13	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	-	1,2,3,5,6,7,8,9,10,14	
Switching Parameters																														
Turn-On Delay	t _{on}	1, 11	-	-	-	12	-	-	-	-	-	12	-	-	ns	Pulse In	Pulse Out	-	-	-	-	-	-	-	4	-	-	14	2,3,5,6,7,8,9,10	
Turn-Off Delay	t _{off}	1, 11	-	-	-	12	-	-	-	-	-	12	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	-	14	2,3,5,6,7,8,9,10	
Rise Time	t _r	1, 11	-	-	-	4.5	-	-	-	-	-	4.5	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	-	14	2,3,5,6,7,8,9,10	
Fall Time	t _f	1, 11	-	-	-	3.0	-	-	-	-	-	3.0	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	-	14	2,3,5,6,7,8,9,10	

*Prime Fan-Out.

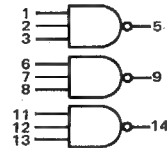
TRIPLE 3-INPUT "NAND" GATE

MTTL II MC2100/2000 series

MC2107 • MC2157
MC2007 • MC2057



This device consists of three 3-Input AND gates driving output inverters. These gates can be used to build a pulse shaping network for interfacing with discrete component circuits.



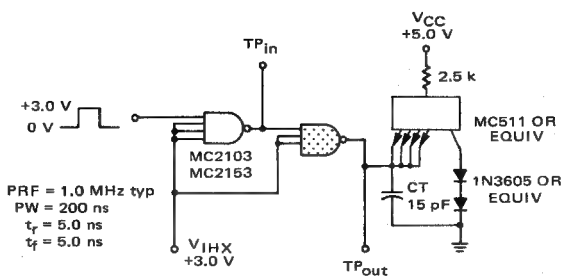
Positive Logic: $5 = \overline{1 \cdot 2 \cdot 3}$
Negative Logic: $5 = \overline{1 + 2 + 3}$

Total Power Dissipation = 66 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

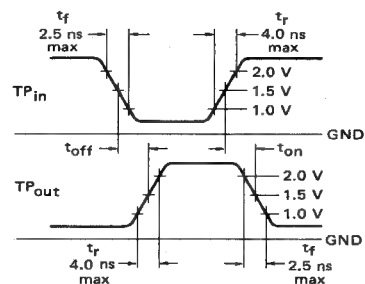
SERIES	INPUT LOADING FACTOR (I_F)	OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
MC2107 MC2157	1 (-2.0 mA)	11 MC2100 series Gates (22 mA) 6 MC2100 series Gates (12 mA)	-55°C to +125°C
MC2007 MC2057	1 (-2.5 mA)	9 MC2000 series Gates (22.5 mA) 5 MC2000 series Gates (12.5 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS

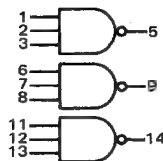


NOTES:
 $R_G = 50 \text{ ohms}$
 C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
Ground inputs to all gates not under test.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



MC2107*, MC2157

MC2007*, MC2057

@ Test Temperature

-55°C
+25°C
+125°C
0°C
+25°C
+75°C

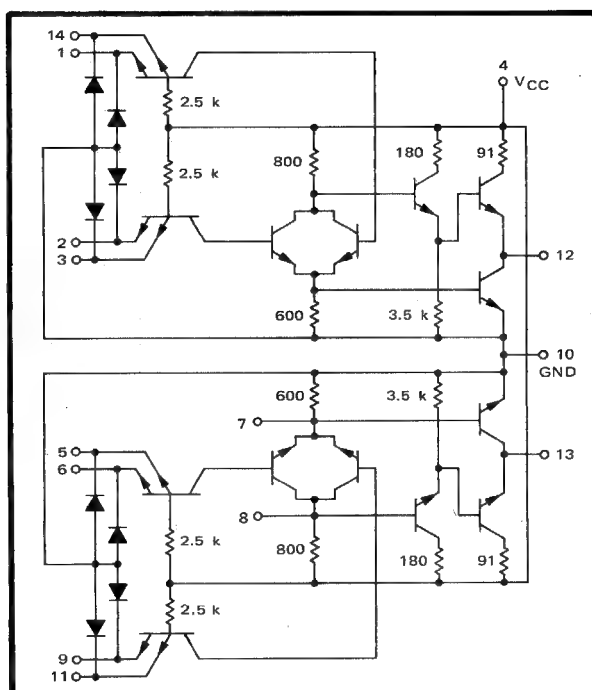
TEST CONDITIONS																Gnd †
mA						Volts										
I _{OL}		I _{OH}		I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}			
Pr*	Std	Pr*	Std													
22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-			
22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0			
22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-			
22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-			
22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0			
22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-			
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																
I _{OL}	I _{OH}	I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}					
-	-	-	-	-	2,3	-	-	-	4	-	-	1,10				
-	-	-	-	-	1	-	-	-	4	-	-	2,3,10				
-	-	-	-	-	1	-	-	-	4	-	-	10				
-	-	1	-	-	-	-	-	-	4	-	-	10				
-	-	1	-	-	-	-	-	-	4	-	-	2,3,10				
5	-	-	-	-	-	1	-	-	4	-	-	10				
-	5	-	-	-	-	-	1	-	4	-	-	10				
-	-	-	-	-	-	-	-	5	4	-	-	1,2,3,10				
-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,10				
5	-	-	-	1	-	-	-	-	4	-	-	10				
-	5	-	1	-	-	-	-	-	4	-	-	10				
-	-	-	-	-	-	-	-	-	-	4	-	1,6,10,11				
-	-	-	-	-	-	-	-	-	4	-	-	10 ‡				
-	-	-	-	-	-	-	-	-	4	-	-	1,6,10,11				
Pulse In	Pulse Out															
1	5	-	-	-	-	-	-	-	4	-	2,3	10				
1	5	-	-	-	-	-	-	-	4	-	2,3	10				
1	5	-	-	-	-	-	-	-	4	-	2,3	10				
1	5	-	-	-	-	-	-	-	4	-	2,3	10				

* Prime Fan-Out † Ground inputs to gates not under test, during ALL tests unless otherwise noted. ‡ The inputs to all gates must be ungrounded.

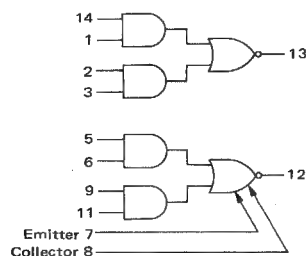
EXPANDABLE DUAL 2-WIDE 2-INPUT "AND-OR-INVERT" GATE

MTTL II MC2100/2000 series

MC2113 • MC2163
MC2013 • MC2063



One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together and driving an output inverter with the ORing nodes made available for expansion. Up to 10 AND gates can be ORed together using the MC2102 or MC2106 expanders series. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



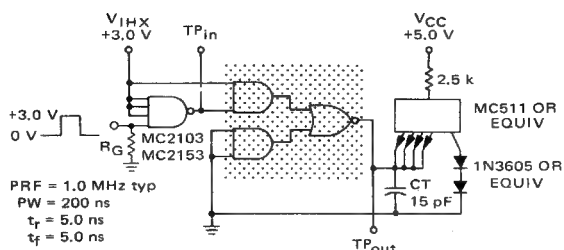
Positive Logic:
13 = (1 · 14) + (2 · 3)
12 = (5 · 6) + (9 · 11) + (Expander)

Total Power Dissipation = 58 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

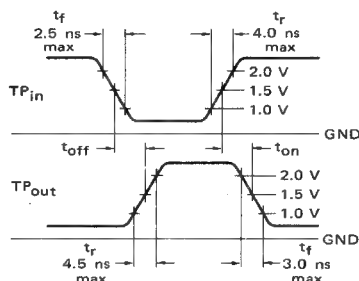
SERIES	INPUT LOADING FACTOR (I _F)	OUTPUT DRIVE (I _{OL})	TEMPERATURE RANGE
MC2113 MC2163	1 (-2.0 mA)	11 MC2100 series Gates (22 mA) 6 MC2100 series Gates (12 mA)	-55°C to +125°C
MC2013 MC2063	1 (-2.5 mA)	9 MC2000 series Gates (22.5 mA) 5 MC2000 series Gates (12.5 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS

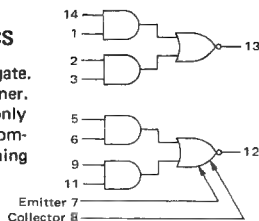


NOTES:
R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
When checking expander side, expander pins should be open.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@ Test Temperature

MC2113*, MC2163

MC2013*, MC2063

		TEST CONDITIONS																		Gnd†
		mA								Volts										
		I _{OL}		I _{OH}		I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}					
		Pr*	Std	Pr*	Std															
22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-							
22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0							
22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-							
22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-							
22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0							
22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-							
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																				
		I _{OL}	I _{OH}	I _{in}	V _{IL}	V _{IH}	V _R	V _{th1}	V _{th0}	V _{out}	V _{CC}	V _{CCH}	V _{IHX}							
Input																				
Forward Current	I _F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	-	-2.5	-	-2.5	-	
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	
Inverse Beta Current	I _L	1	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-	
Breakdown Voltage	BV _{in "0"}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	
	BV _{in "1"}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	
Output																				
Output Voltage	V _{out "0"}	13	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	
	V _{out "1"}	13	2.5	-	2.4	-	2.5	-	2.4	-	2.5	-	2.4	-	2.5	-	2.4	-	2.5	
Leakage Current	I _{OLK}	13	-	250	-	250	-	250	-	250	-	250	-	250	-	250	-	250	-	
Short-Circuit Current	I _{SC}	13	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-	
Output Voltage	V _{OL}	13	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	
	V _{OH}	13	2.7	-	3.1	-	3.15	-	2.9	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	
Power Requirements																				
(Total Device)																				
Maximum Power Supply Current	I _{max}	4	-	-	-	20	-	-	-	-	-	22	-	-	-	-	-	-	-	
Power Supply Drain	I _{PDH}	4	-	18	-	18	-	18	-	24	-	24	-	24	-	24	-	24	-	
	I _{PDL}	4	-	12	-	12	-	12	-	15	-	15	-	15	-	15	-	15	-	
Switching Parameters																				
Turn-On Delay	t _{on}	1, 13	-	-	-	11	-	-	-	-	-	11	-	-	-	-	-	-	-	
Turn-Off Delay	t _{off}	1, 13	-	-	-	11	-	-	-	-	-	11	-	-	-	-	-	-	-	
Rise Time	t _r	1, 13	-	-	-	4.5	-	-	-	-	-	4.5	-	-	-	-	-	-	-	
Fall Time	t _f	1, 13	-	-	-	3.0	-	-	-	-	-	3.0	-	-	-	-	-	-	-	

* Prime Fan-Out

† Ground inputs to gates not under test during ALL tests unless otherwise noted.

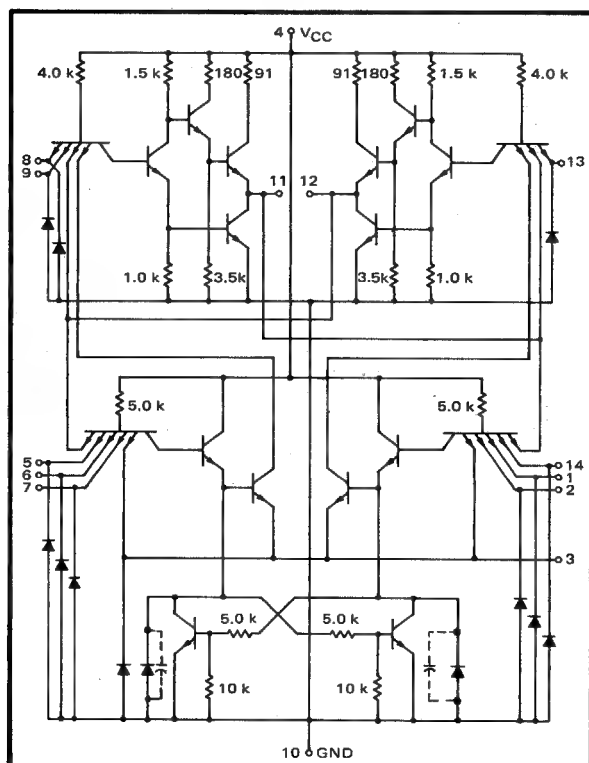
‡ The inputs to all gates must be ungrounded.

MC2113, MC2163/MC2013, MC2063 (continued)

"AND" J-K FLIP-FLOP

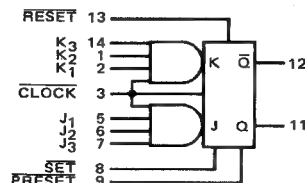
MTTL II MC2100/2000 series

MC2109 • MC2159 MC2009 • MC2059

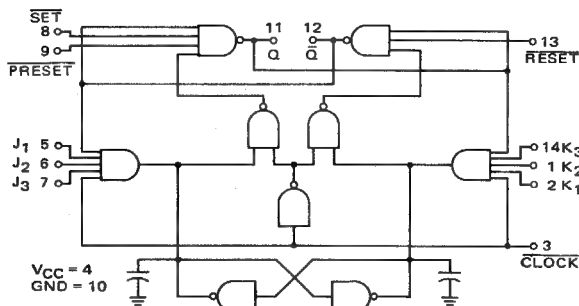


The MC2009, MC2059, MC2109, and MC2159 are clocked flip-flops that trigger on the negative edge and perform the J-K logic junction. Each flip-flop has an AND input gating configuration consisting of three J inputs ANDed together and three K inputs ANDed together. The multiple J and K inputs minimize the requirements for external gates in counters and certain other applications. A direct SET, PRESET, and RESET are also available.

In normal operation, information is changed on the J and K inputs while the clock is in a low state, since the inputs are inhibited in this condition. Information is read into a temporary memory when the clock is in a high state. When the clock returns low, the information is transferred to the bi-stable section and the Q and \bar{Q} outputs respond accordingly. The information on the J and K inputs should not be changed while the clock is high. Each flip-flop can be set or reset directly by the direct SET, PRESET, or RESET inputs. Since each flip-flop is a charge-storage device, there is a restriction on the clock fall time that must be observed.



EQUIVALENT CIRCUIT



J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$$\text{Where } J = J_1 \cdot J_2 \cdot J_3 \\ K = K_1 \cdot K_2 \cdot K_3$$

Total Power Dissipation = 40 mW typ/Pkg

Switching Times:

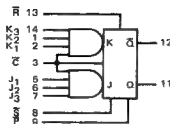
$t_{on} = 20 \text{ ns typ}$

$t_{off} = 13 \text{ ns typ}$

SERIES	INPUT LOADING FACTOR (I_F)				OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
	CLOCK	ALL OTHER	CLOCK	ALL OTHER		
MC2109 MC2159	1.00	0.66	(-2.0 mA)	(-1.33 mA)	11 MC2100 series Gates (22.0 mA) 6 MC2100 series Gates (12.0 mA)	-55°C to +125°C
MC2009 MC2059	1.00	0.66	(-2.5 mA)	(-1.66 mA)	9 MC2000 series Gates (22.5 mA) 5 MC2000 series Gates (12.5 mA)	0°C to +75°C

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and K input, plus the SET, PRESET, and RESET inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



@ Test
Temperature

MC2109*, MC2159
-55°C
+25°C
+125°C
MC2009*, MC2059
0°C
+25°C
+75°C

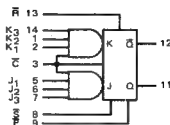
		TEST CONDITIONS												TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:										Gnd	
		mA						Volts																	
		I_{OL}		I_{OH}		I_{in}	$2 I_{in}$	V_{IL}	V_{IH}	V_R	V_{th0}	V_{th1}	V_{out}												V_{CC}
		Pr*	Std	Pr*	Std																				
		22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.0	2.0	5.5	5.0											
		22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.2	1.7	5.5	5.0											
		22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	0.9	1.4	5.5	5.0											
		22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.9	5.5	5.0											
		22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.2	1.8	5.5	5.0											
		22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.7	5.5	5.0											
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																									
		I_{OL}	I_{OH}	I_{in}	$2 I_{in}$	V_{IL}	V_{IH}	V_R	V_{th0}	V_{th1}	V_{out}	V_{CC}	Gnd												
c	-	-	-	-	-	-	-	2,3,5,6, 7,9,13,14	-	-	-	4	1,8,10												
	-	-	-	-	-	-	-	1,2,3,6, 7,8,9,14	-	-	-	↓	5,10,13												
	-	-	-	-	-	-	-	1,2,3,5, 6,7,9,14	-	-	-	↓	8,10,13												
	-	-	-	-	-	-	-	1,2,3,5, 6,7,8,14	-	-	-	↓	9,10,13												
	-	-	-	-	-	-	-	1,2,3,5, 6,7,9,14	-	-	-	↓	8,10,13												
c	-	-	-	-	-	-	-	1	-	-	-	4	2,3,5,6,7,10,11,14												
	-	-	-	-	-	-	-	5	-	-	-	↓	1,2,3,6,7,10,12,14												
	-	-	-	-	-	-	-	8	-	-	-	↓	1,2,3,5,6,7,9,10,12,14												
	-	-	-	-	-	-	-	9	-	-	-	↓	1,2,3,5,6,7,8,10,12,14												
	-	-	-	-	-	-	-	13	-	-	-	↓	1,2,3,5,6,7,10,11,14												
c	-	-	-	-	8	-	1	-	-	-	-	4	10												
	-	-	-	-	13	-	5	-	-	-	-	↓	↓												
	-	-	-	-	↓	-	8	-	-	-	-	↓	↓												
	-	-	-	-	8	-	9	-	-	-	-	↓	↓												
	-	-	-	-	↓	-	13	-	-	-	-	↓	↓												
c	-	-	-	1	-	8	-	-	-	-	-	4	10												
	-	-	-	5	-	13	-	-	-	-	-	↓	↓												
	-	-	-	8	-	↓	-	-	-	-	-	↓	↓												
	-	-	-	9	-	↓	-	-	-	-	-	↓	↓												
	-	-	-	13	-	↓	-	-	-	-	-	↓	↓												
c	-	-	-	1	-	-	-	-	-	-	-	4	2,3,5,6,7,10,11,14												
	-	-	-	5	-	-	-	-	-	-	-	↓	1,2,3,6,7,10,12,14												
	-	-	-	8	-	-	-	-	-	-	-	↓	1,2,3,5,6,7,9,10,12,14												
	-	-	-	9	-	-	-	-	-	-	-	↓	1,2,3,5,6,7,8,10,12,14												
	-	-	-	13	-	-	-	-	-	-	-	↓	1,2,3,5,6,7,10,11,14												

* Prime Fan-Out.

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Test procedures are shown for only one J and K input, plus the SET, PRESET, and RESET inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



@ Test
Temperature

MC2109*, MC2159

MC2009*, MC2059

-55°C
+25°C
0°C
+25°C
+75°C

														TEST CONDITIONS														
														mA					Volts									
														I_{OL}		I_{OH}		I_{in}		$2 I_{in}$	V_{IL}	V_{IH}	V_R	V_{th0}	V_{th1}	V_{out}	V_{CC}	
														Pr*	Std	Pr*	Std	I_{in}	$2 I_{in}$	V_{IL}	V_{IH}	V_R	V_{th0}	V_{th1}	V_{out}	V_{CC}		
														22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.0	2.0	5.5	5.0		
														22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.2	1.7	5.5	5.0		
														22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	0.9	1.4	5.5	5.0		
														22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.9	5.5	5.0		
														22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.2	1.8	5.5	5.0		
														22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.7	5.5	5.0		
														TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:														
														I_{OL}	I_{OH}	I_{in}	$2 I_{in}$	V_{IL}	V_{IH}	V_R	V_{th0}	V_{th1}	V_{out}	V_{CC}	Gnd			
Clock Input																												
Forward Current	I_F	3	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-	-	-	-	-	-	-	1,2,5,6, 7,8,9,13,14	-	-	-	-	4	3,10	
Leakage Current	I_R	3	-	150	-	150	-	150	-	150	-	150	-	-	-	-	-	-	-	-	3	-	-	-	-	4	1,2,5,6,7,10,14	
Inverse Beta Current	I_L	3	-	200	-	200	-	200	-	200	-	200	-	-	-	-	-	-	-	-	3	-	-	-	-	4	10	
		3	-	200	-	200	-	200	-	200	-	200	-	-	-	-	-	-	-	-	3	-	-	-	-	4	10	
Breakdown Voltage	$BV_{in"0"}$	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	-	-	-	3	13	-	-	-	-	-	-	4	10	
		3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	-	-	-	3	8	-	-	-	-	-	-	4	10	
	$BV_{in"1"}$	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	-	-	-	3	-	-	-	-	-	-	-	4	1,2,5,6,7,10,14	
Output																												
Output Voltage	$V_{out"0"}$	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	12	-	-	-	-	-	-	-	-	13	-	-	4	3,8,10	
		11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	9	-	-	-	3,10,13		
		11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	8	-	-	-	3,10,13		
	$V_{out"1"}$	12	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	-	12	-	-	-	-	-	13	-	-	-	4	8,10	
		11	-	-	-	-	-	-	-	-	-	-	-	-	11	-	-	-	-	-	-	9	-	-	-	10,13		
		11	-	-	-	-	-	-	-	-	-	-	-	-	11	-	-	-	-	-	-	8	-	-	-	10,13		
Leakage Current	I_{OLK}	12	-	225	-	225	-	225	-	225	-	225	-	-	-	-	-	-	-	-	-	-	-	12	4	1,2,3,5,6,7,8,9,10,13,14		
		11	-	225	-	225	-	225	-	225	-	225	-	-	-	-	-	-	-	-	-	-	-	11	4	1,2,3,5,6,7,8,9,10,13,14		
Short-Circuit Current	I_{SC}	12	-	-30	-	-70	-	-	-	-30	-	-70	-	-	-	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,9,10,12,13,14	
		11	-	-30	-	-70	-	-	-	-30	-	-70	-	-	-	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,9,10,11,13,14	
Output Voltage	V_{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	12	-	-	-	-	13	-	-	-	-	-	-	4	3,8,10	
		11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	3,10,13		
		11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	3,10,13		
	V_{OH}	12	2.80	-	3.20	-	3.35	-	3.00	-	3.10	-	3.15	-	-	12	-	13	-	-	-	-	-	-	-	4	8,10	
		11	-	-	-	-	-	-	-	-	-	-	-	-	11	-	9	-	-	-	-	-	-	-	-	10,13		
		11	-	-	-	-	-	-	-	-	-	-	-	-	11	-	8	-	-	-	-	-	-	-	-	10,13		
Power Requirements (Total Device)																												
Power Supply Drain	I_{PD}	4	-	12	-	12	-	12	-	14	-	14	-	14	-	-	-	-	-	-	-	-	-	-	-	4	3,10,13	
	I_{PD}	4	-	12	-	12	-	12	-	14	-	14	-	14	-	-	-	-	-	-	-	-	-	-	-	4	3,8,10	

* Prime Fan-Out.

OPERATING CHARACTERISTICS

Clock fall time ≤ 100 ns.

Triggers on clock pulse widths ≥ 15 ns.

Provides direct $\overline{\text{SET}}$, $\overline{\text{PRESET}}$, and $\overline{\text{RESET}}$ inputs. The application of a "0" state to 8 or 9, sets Q high; "0" state to 13, resets Q low. The clock must be in the low state when these functions are performed.

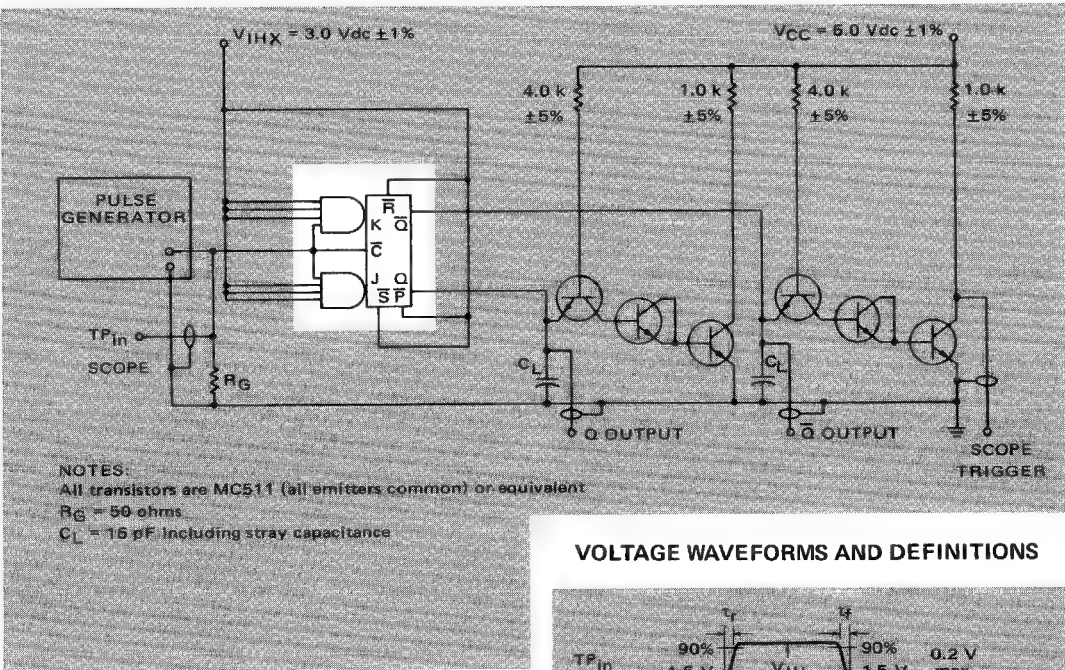
Data at the J and K inputs must be present before the clock goes to a high state. If the information on the J and K inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1"

state to "0" state information change on the J and K terminals. The flip-flop will require typically 6.0 ns to recognize a "0" state to "1" state change.

Negative edge triggering — When the clock goes from the high state to the low state, the information in the temporary storage section is transferred and the Q and $\overline{\text{Q}}$ outputs will respond accordingly. While the clock is in a low state, the J and K terminals are inhibited.

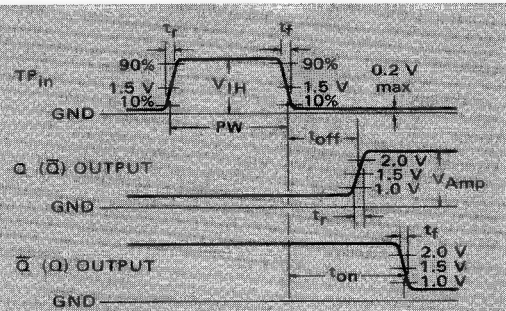
Unused J and K inputs should be tied to the clock or to 2.0 to 5.0 Vdc. $\overline{\text{PRESET}}$ and $\overline{\text{SET}}$ are tied to $\overline{\text{Q}}$; $\overline{\text{RESET}}$ is tied to Q.

FIGURE 1 — SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



NOTES:
All transistors are MC511 (all emitters common) or equivalent
 $R_G = 50$ ohms
 $C_L = 16$ pF, including stray capacitance

VOLTAGE WAVEFORMS AND DEFINITIONS



SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	t_{off}	V		20	ns
Delay Time On	t_{on}	V		25	ns
Rise Time	t_r	V		6.0	ns
Fall Time	t_f	V		4.0	ns
Amplitude	V_{Amp}	V	3.2		Volt
WORST-CASE TESTS (Device must toggle with each clock pulse)					
TEST	SYMBOL	LIMITS	INPUT CONDITIONS		
Toggle Frequency	f_{Tog}	30 MHz max	W		
Pulse Width	PW	15 ns min	X		
Input High Voltage	V_{IH}	1.8 V min	Y		
Fall Time	t_f	100 ns max	Z		

INPUT PULSE CONDITIONS

SYMBOL	W	V	X	Y	Z	UNIT
PRF	30	5.0	5.0	5.0	1.0	MHz
PW	15	100	15	100	200	ns
t_r	≤ 10	≤ 10	≤ 10	≤ 10	≤ 50	ns
t_f	≤ 10	≤ 10	≤ 10	≤ 10	100	ns
V_{IH}	3.5	3.5	3.5	1.8	3.5	Volt

FIGURE 2 – J-K TERMINAL CHARACTERISTICS TEST CIRCUIT

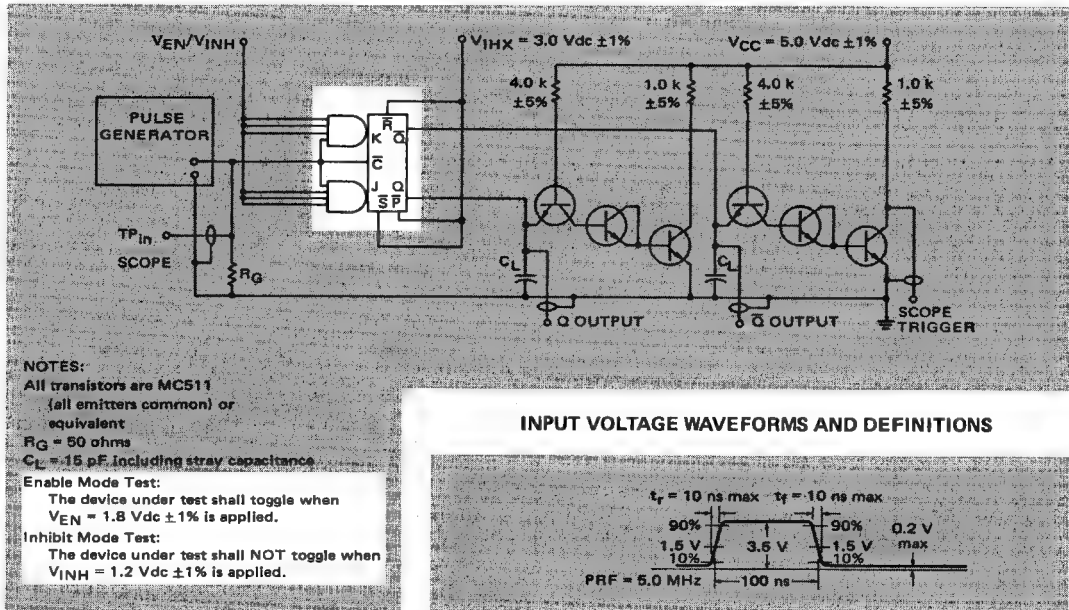
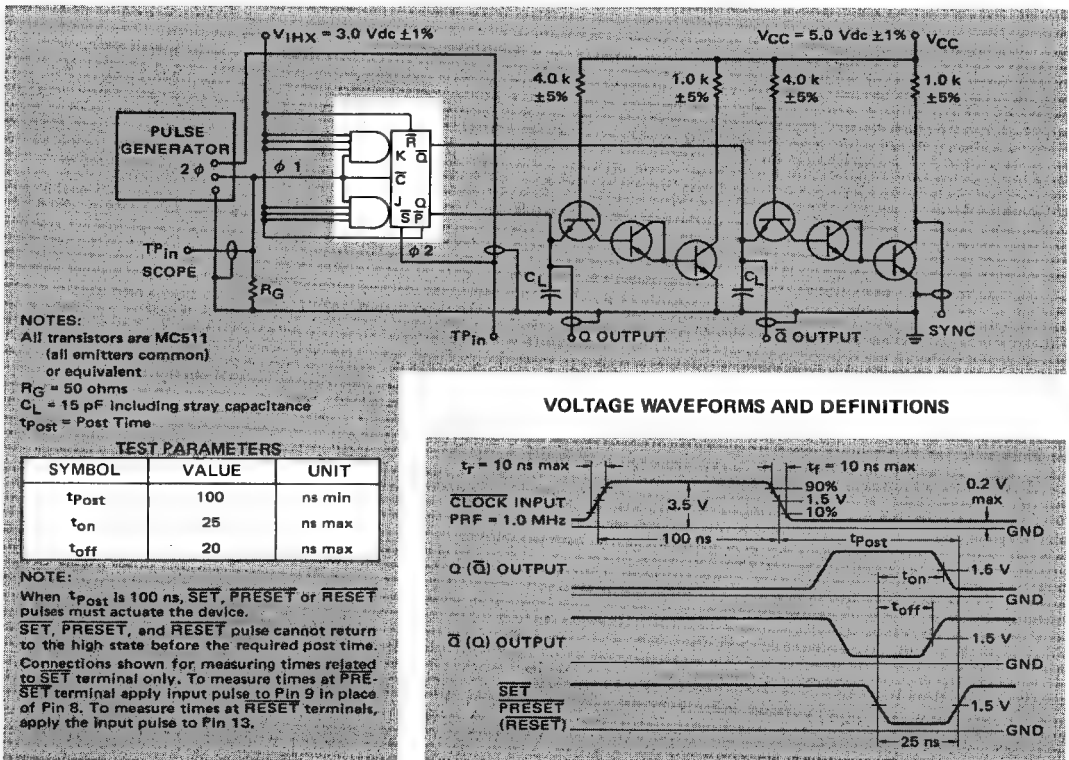


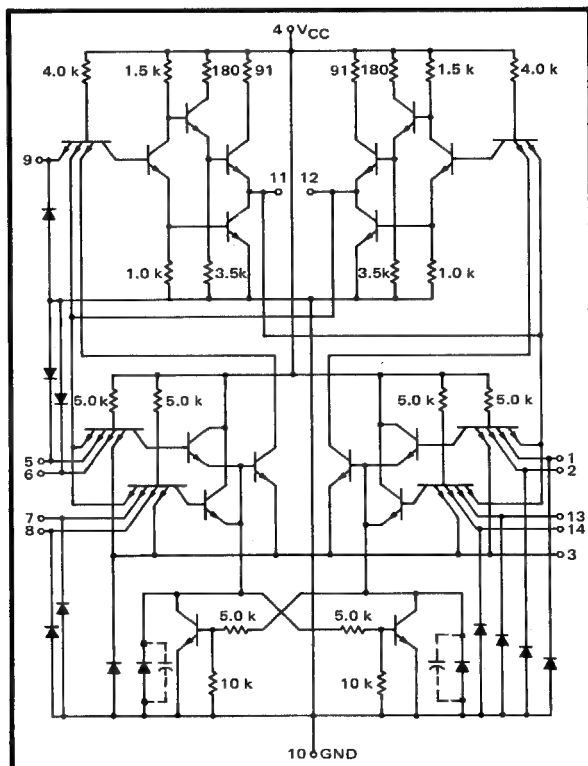
FIGURE 3 – SET-RESET-PRESET TERMINAL CHARACTERISTICS TEST CIRCUIT



"OR" J-K FLIP-FLOP

MTTL II MC2100/2000 series

MC2110 • MC2160 MC2010 • MC2060

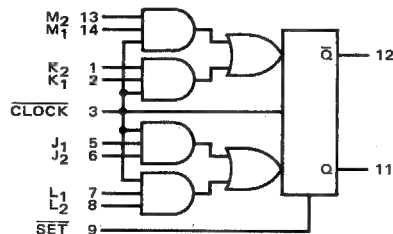


The MC2110, MC2160, MC2010, and MC2060 are clocked flip-flops that trigger on the negative edge and are internally wired to perform the J-K logic function. Each flip-flop has a positive logic AND-OR input gating configuration that consists of two clocked J inputs ANDed together, two clocked K inputs ANDed together, two clocked L inputs ANDed together, and two clocked M inputs ANDed together. The J and the L inputs are ORed together and the K and the M inputs are ORed together. A direct SET is also available.

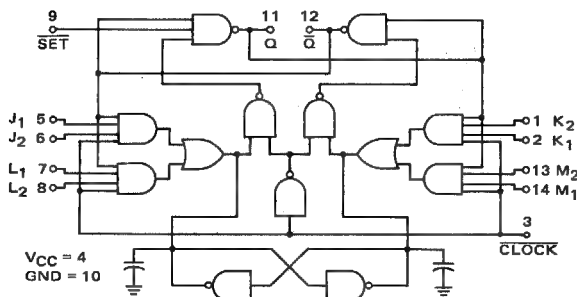
In normal operation, information is changed on the clocked inputs while the clock is in a low state, since the inputs are inhibited in this condition. Information is read into a temporary memory through the AND-OR input gating when the clock is in the high state. When the clock returns low the information in the temporary memory is transferred to the bi-stable section and the Q and the \bar{Q} outputs respond accordingly. The information on the clocked inputs should not be changed while the clock is high.

Each flip-flop can be set directly by applying a low state to the direct SET input. Since each flip-flop is a charge storage device there is a restriction on the clock fall time that must be observed.

The AND-OR input configuration of each flip-flop makes it very useful for shift right/shift left registers and for up/down counters.



EQUIVALENT CIRCUIT



J	L	K	M	Q_n	Q_{n+1}
0	0	X	X	0	0
1	X	X	X	0	1
X	1	X	X	0	1
X	X	0	0	1	1
X	X	1	X	1	0
X	X	X	1	1	0

X = Don't Care
Where $J = J_1 \cdot J_2$
 $L = L_1 \cdot L_2$
 $K = K_1 \cdot K_2$
 $M = M_1 \cdot M_2$

Total Power Dissipation = 50 mW typ/Pkg

Switching Times:

$t_{on} = 20$ ns typ

$t_{off} = 13$ ns typ

SERIES	INPUT LOADING FACTOR		(If)		OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
	CLOCK	ALL OTHER	CLOCK	ALL OTHER		
MC2110 MC2160	2.00	0.66	(-4.0 mA)	(-1.33 mA)	11 MC2100 series Gates (22.0 mA) 6 MC2100 series Gates (12.0 mA)	-55°C to +125°C
MC2010 MC2060	2.00	0.66	(-5.0 mA)	(-1.66 mA)	9 MC2000 series Gates (22.5 mA) 5 MC2000 series Gates (12.5 mA)	0°C to +75°C

MC2110*, MC2160

MC2010*, MC2060

$$\begin{array}{l} 160 \left\{ \begin{array}{l} -55^{\circ}\text{C} \\ +25^{\circ}\text{C} \\ +125^{\circ}\text{C} \end{array} \right. \\ 060 \left\{ \begin{array}{l} 0^{\circ}\text{C} \\ +25^{\circ}\text{C} \\ +75^{\circ}\text{C} \end{array} \right. \end{array}$$

TEST CONDITIONS													Gnd	
mA						Volts								
I_{OL}		I_{OH}		I_{in}	$2 I_{in}$	$4 I_{in}$	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}		V_{CC}
Pr*	Std	Pr*	Std											
22.0	12.0	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	
22.0	12.0	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	
22.0	12.0	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	
22.5	12.5	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	
22.5	12.5	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	
22.5	12.5	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:														
I_{OL}	I_{OH}	I_{in}	$2 I_{in}$	$4 I_{in}$	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{CC}	Gnd		
-	-	-	-	-	-	-	2,3,5,6,7,8,13,14	-	-	-	4	1,9,10		
-	-	-	-	-	-	-	1,2,3,6,7,8,13,14	-	-	-	↓	5,10,11		
-	-	-	-	-	-	-	1,2,5,6,7,8,13,14	-	-	-	↓	3,9,10,11		
-	-	-	-	-	-	-	1	-	-	-	4	2,3,5,6,7,8,10,11,13,14		
-	-	-	-	-	-	-	5	-	-	-	↓	1,2,3,6,7,8,9,10,12,13,14		
-	-	-	-	-	-	-	9	-	-	-	↓	1,2,3,5,6,7,8,10,12,13,14		
-	-	-	-	-	-	-	1	-	-	-	4	9,10		
-	-	-	-	-	-	-	5	-	-	-	↓	10,11		
-	-	-	-	-	-	-	9	-	-	-	↓	10,11		
-	-	1	-	-	-	-	-	-	-	-	4	9,10		
-	-	5	-	-	-	-	-	-	-	-	↓	10,11		
-	-	9	-	-	-	-	-	-	-	-	↓	10,11		
-	-	1	-	-	-	-	-	-	-	-	4	2,3,5,6,7,8,10,11,13,14		
-	-	5	-	-	-	-	-	-	-	-	↓	1,2,3,6,7,8,9,10,12,13,14		
-	-	9	-	-	-	-	-	-	-	-	↓	1,2,3,5,6,7,8,10,12,13,14		
-	-	-	-	-	-	-	1,2,5,6,7,8,13,14	-	-	-	4	3,10		
-	-	-	-	-	-	-	3	-	-	-	4	1,2,5,6,7,8,10,13,14		
-	-	-	-	-	-	-	3	-	-	-	4	9,10		
-	-	-	-	-	-	-	3	-	-	-	4	10,11		
-	-	-	-	3	-	-	-	-	-	-	4	10,11		
-	-	-	-	3	-	-	-	-	-	-	4	10,12		
-	-	-	3	-	-	-	-	-	-	-	4	1,2,5,6,7,8,10,13,14		
11⊙	-	-	-	-	-	-	-	9	-	-	4	3,10		
-	11	-	-	-	-	-	-	-	9	-	4	3,10		
-	-	-	-	-	-	-	12	-	-	-	4	1,2,3,5,6,7,8,10,11,13,14		
-	-	-	-	-	-	-	11	-	-	-	4	1,2,3,5,6,7,8,9,10,13,14		
-	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,10,11,12,13,14		
-	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,9,10,11,13,14		
-	12	-	-	-	-	-	-	-	-	-	4	3,10,11		
-	11	-	-	-	-	-	-	-	-	-	4	3,10,12		
12⊙	-	-	-	-	-	9	-	-	-	-	4	3,10		
11⊙	-	-	-	-	-	9	-	-	-	-	4	3,10		
-	-	-	-	-	-	-	-	-	-	12	4	1,2,3,5,6,7,8,10,11,13,14		
-	-	-	-	-	-	-	-	-	-	11	4	1,2,3,5,6,7,8,9,10,13,14		
-	-	-	-	-	-	-	-	-	-	-	4	3,10,12		
-	-	-	-	-	-	-	-	-	-	-	4	3,10,11		

MC2110, MC2160/MC2010, MC2060 (continued)

MC2110, MC2160/MC2010, MC2060(continued)

OPERATING CHARACTERISTICS

Clock fall time ≤ 100 ns.

Triggers on clock pulse widths ≥ 15 ns.

The application of a "0" state to the $\overline{\text{SET}}$ will cause Q to go to the "1" state. The clock must be in the low state when this function is performed.

Data at the clocked inputs must be present before the clock goes to a high state. If the information on the clocked inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1" state to "0" state change. The flip-flop will also require typically 6.0 ns to recognize a "0" state to "1" state change.

Negative edge triggering — When the clock goes from the high state, the information in the temporary storage section is transferred; and the Q and $\overline{\text{Q}}$ outputs will change accordingly. While the clock is in a low state, the J, K, L, and M terminals are inhibited.

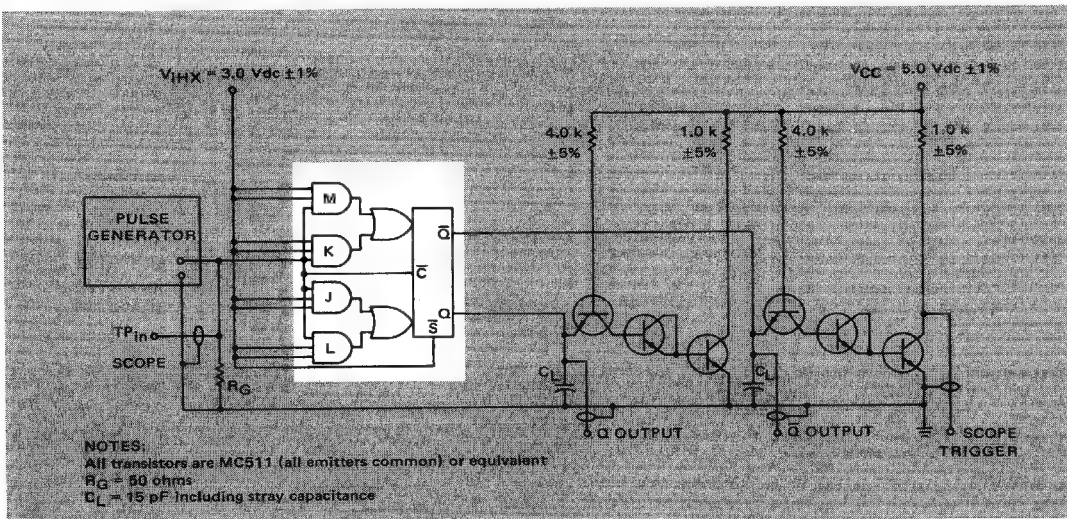
Unused Inputs:

Single unused J, K, L, and M inputs should be tied to the used input, to the clock input, or to 2.0 to 5.0 Vdc.

If both J, K, L, or M inputs are unused, they MUST be tied to ground.

Unused $\overline{\text{SET}}$ is tied to $\overline{\text{Q}}$.

FIGURE 1 — SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



VOLTAGE WAVEFORMS AND DEFINITIONS

SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	t_{off}	V		20	ns
Delay Time On	t_{on}	V		25	ns
Rise Time	t_r	V		6.0	ns
Fall Time	t_f	V		4.0	ns
Amplitude	V_{amp}	V	3.2		Volt
WORST-CASE TESTS (Device must toggle with each clock pulse)					
TEST	SYMBOL	LIMITS	INPUT CONDITIONS		
Toggle Frequency	f_{Tog}	30 MHz max	W		
Pulse Width	PW	15 ns min	X		
Input High Voltage	V_{IH}	1.8 V min	Y		
Fall Time	t_f	100 ns max	Z		

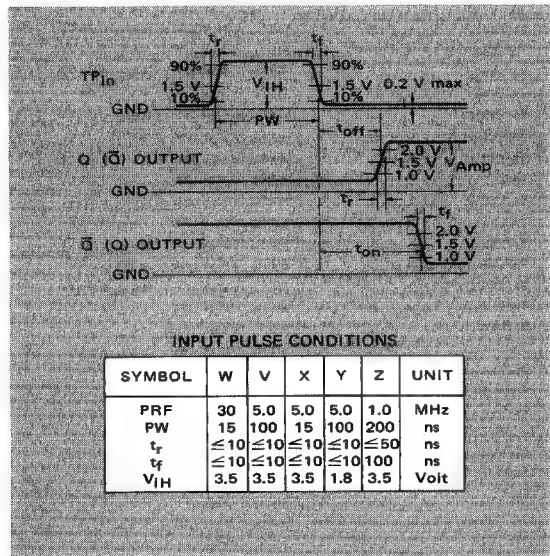
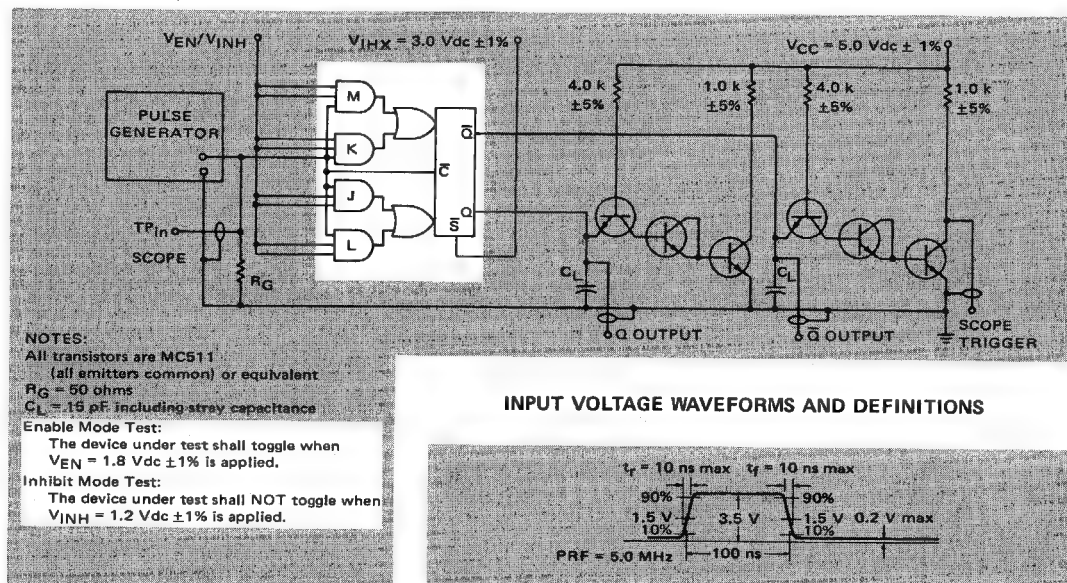
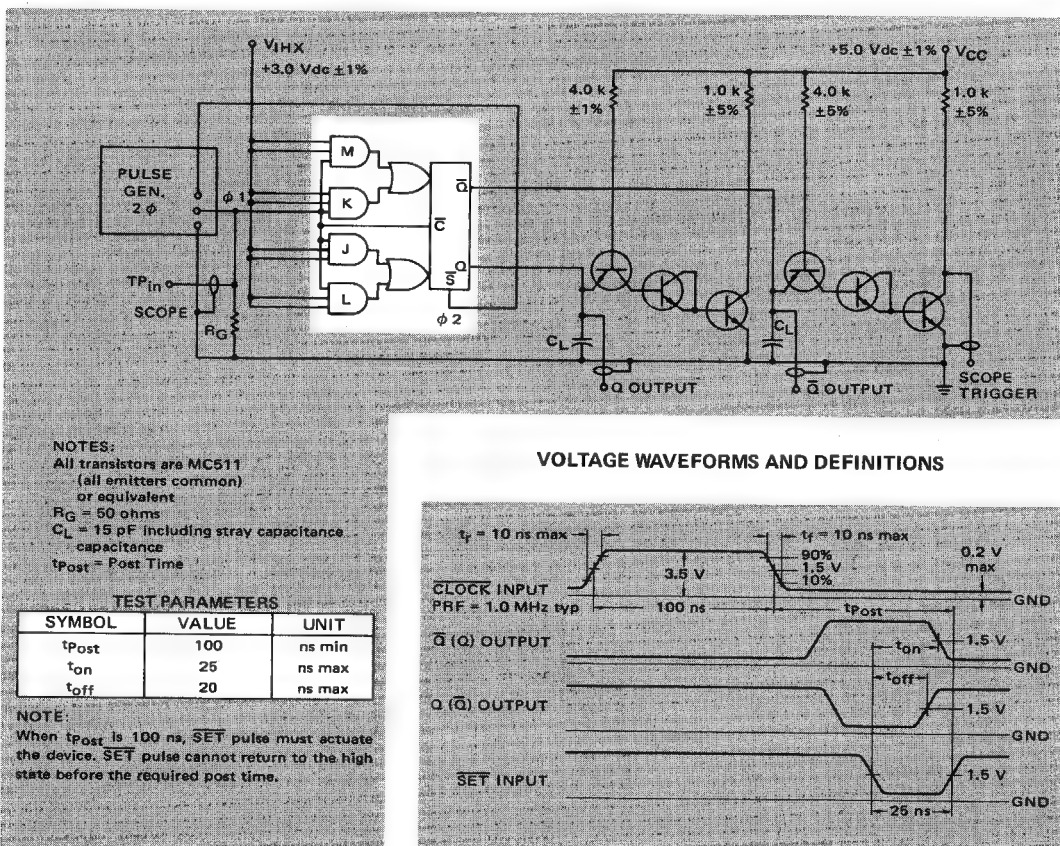


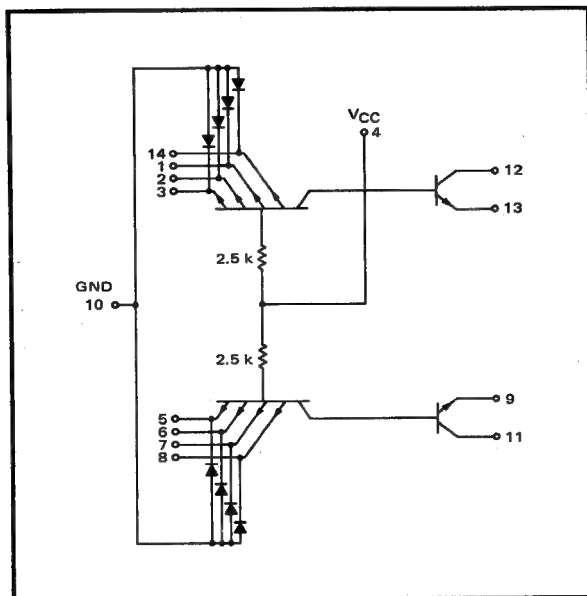
FIGURE 2 – J-K-L-M TERMINAL CHARACTERISTICS TEST CIRCUIT


FIGURE 3 – $\overline{\text{SET}}$ TERMINAL CHARACTERISTICS TEST CIRCUIT


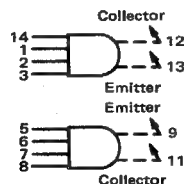
DUAL 4-INPUT EXPANDER FOR "AND-OR-INVERT" GATES

MTTL II MC2100/2000 series

**MC2106 • MC2156
MC2006 • MC2056**



This device consists of two independent 4-input AND gates. The outputs of each gate are made available as ORing nodes. Using the MC2102 series and the MC2106 series with any one of the basic expandable gates, up to 10 AND gates can be ORed together.



Total Power Dissipation = 14 mW typ/Pkg.

Propagation Delay Times:

$\Delta t_{pd} = +1.0$ ns typ

When added to the expandable AND-OR-INVERT gates.

$\Delta t_{pd}/pF = +0.7$ ns/pF typ

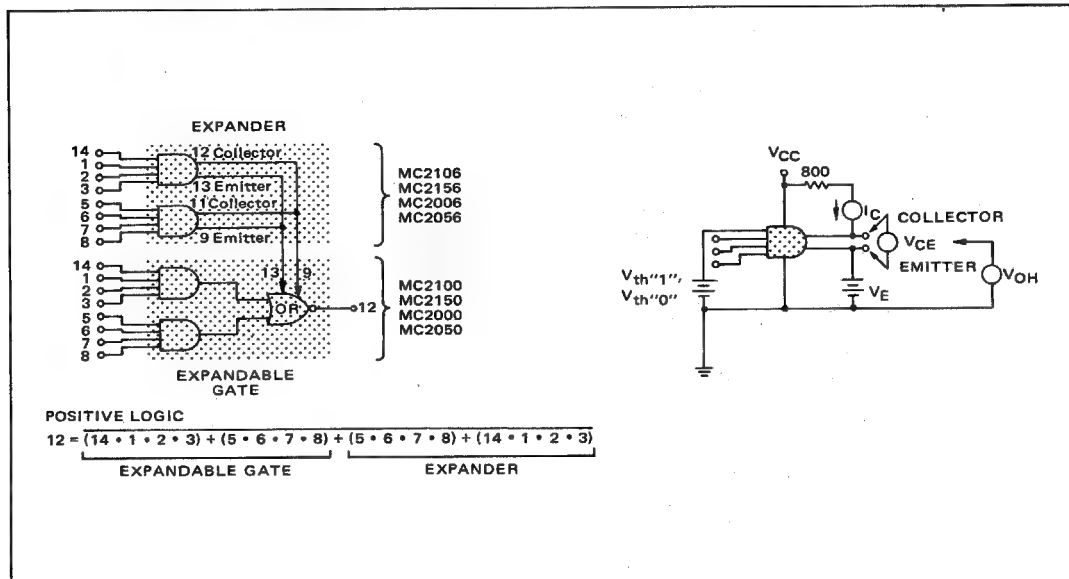
Caused by additional capacitance at expansion points.

SERIES	INPUT LOADING FACTOR	(I_F)	TEMPERATURE RANGE
MC2106 MC2156	1	-2.0 mA	-55°C to +125°C
MC2006 MC2056	1	-2.5 mA	0°C to +75°C

Full output loading factor of the expandable gate is maintained.

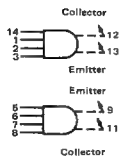
APPLICATION: EXPANDABLE 2-WIDE 4-INPUT, "AND-OR-INVERT" GATE WITH A DUAL 4-INPUT EXPANDER CONNECTED.

V_{CE} , V_{OH} TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



@ Test
Temperature

MC2106, MC2156

-55°C

+25°C

+125°C

MC2006, MC2056

0°C

+25°C

+75°C

Characteristic	Symbol	Pin Under Test	MC2106, MC2156 Test Limits						MC2006, MC2056 Test Limits						Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:														Gnd†
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C			I _C	I _{in}	V _R	V _{E1}	V _{E2}	V _{E3}	V _{th1}	V _{th0}	V _{out}	V _{CR}	V _{CRH}	V _{CC}	V _{CCH}		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max																
Input																														
Forward Current	I _F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	2,3,14	-	-	-	-	-	-	-	-	-	4	-	1,10
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	-	-	-	-	-	-	-	-	-	4	-	2,3,10,14
Inverse Beta Current	I _L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	13	-	-	-	-	-	-	12	-	4	-	10
Breakdown Voltage	BV _{in"0"}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	13	-	-	-	-	-	-	12	-	4	-	10
	BV _{in"1"}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	-	4	-	2,3,10,14
Output																														
Output Voltage	V _{OH}	12	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	Vdc	-	-	-	-	13	-	-	1	-	12	-	4	-	10	
	V _{CE} ①	12	-	0.65	-	0.65	-	0.65	-	0.65	-	0.65	-	0.65	Vdc	12	-	-	13	-	-	1	-	-	-	-	4	-	10	
Leakage Current	I _{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	13	-	-	12	-	-	4	-	1,2,3,10,14	
Power Requirements (Total Device)																														
Maximum Power Supply Current	I _{max} ②	4	-	-	-	7.0	-	-	-	-	-	-	7.5	-	mAdc	-	-	-	-	-	9,13	-	-	-	-	11, 12	-	4	1,2,3,10,14	
Power Supply Drain	I _{PDH}	4	-	3.0	-	3.0	-	3.0	-	3.6	-	3.6	-	3.6	mAdc	-	-	-	-	-	9,13	-	-	-	-	-	4	-	10‡	
	I _{PDL}	4	-	4.25	-	4.25	-	4.25	-	5.25	-	5.25	-	5.25	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,10,14	

* Indicated pins tied to V_{CC} thru 800 ohms ± 1.0% resistor.

** Indicated pins tied to V_{CCH} thru 800 ohms ± 1.0% resistor.

† Ground inputs to gate not under test during ALL tests, unless otherwise noted.

‡ The inputs of both gates must be ungrounded.

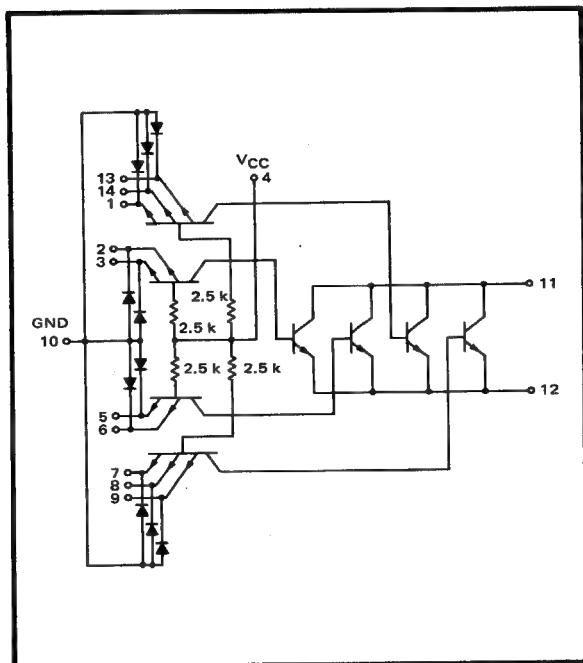
① V_{CE} is referenced to the emitter voltage (Pin 13). The other gate is referenced to (Pin 9).

② Pin 9 ties to Pin 13. Pin 12 ties to Pin 11.

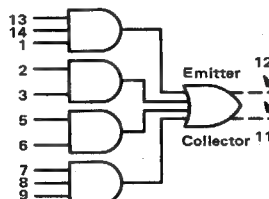
4-WIDE 3-2-2-3 INPUT EXPANDER FOR "AND-OR-INVERT" GATES

MTTL II MC2100/2000 series

MC2102 • MC2152
MC2002 • MC2052



This device consists of two 2-input and two 3-input AND gates ORED together with the common ORing nodes made available as the output. The basic expandable gate can be expanded up to 10 AND gates by using the MC2102 series or the MC2106 series expander package.



Total Power Dissipation = 28 mW typ/Pkg.

Propagation Delay Times:

$\Delta t_{pd} = +2.0$ ns typ

When added to the expandable
AND-OR-INVERT gates.

$\Delta t_{pd}/pF = +0.7$ ns/pF typ

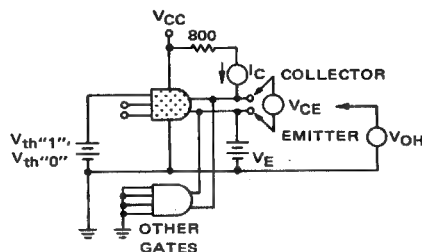
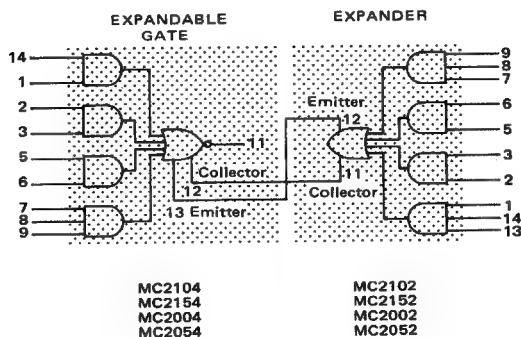
Caused by additional capacitance
at expansion points.

SERIES	INPUT LOADING FACTOR	(I _F)	TEMPERATURE RANGE
MC2102 MC2152	1	-2.0 mA	-55°C to +125°C
MC2002 MC2052	1	-2.5 mA	0°C to +75°C

Full output loading factor of the expandable gate is maintained.

**APPLICATION: EXPANDABLE 4-WIDE "AND-OR-INVERT"
GATE WITH A 4-WIDE 3-2-2-3 INPUT EX-
PANDER CONNECTED.**

V_{CE}, V_{OH} TEST CIRCUIT

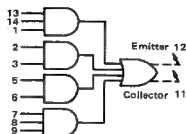


EXPANDER (MC2102)
POSITIVE LOGIC

$$11 = \underbrace{(13 \cdot 14 \cdot 1) + (2 \cdot 3) + (5 \cdot 6) + (7 \cdot 8 \cdot 9)}_{\text{EXPANDER}} + \underbrace{(14 \cdot 1) + (2 \cdot 3) + (5 \cdot 6) + (7 \cdot 8 \cdot 9)}_{\text{EXPANDABLE GATE}}$$

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.



@ Test Temperature

MC2102, MC2152 {
 -55°C
 +25°C
 +125°C

MC2002, MC2052 {
 0°C
 +25°C
 +75°C

TEST CONDITIONS															
mA		Volts													
I _C	I _{in}	V _R	V _{E1}	V _{E2}	V _{E3}	V _{th1}	V _{th0}	V _{out}	V _{CR}	V _{CRH}	V _{CC}	V _{CCH}			
6.0	1.0	4.5	1.00	0.90	0.8	2.0	0.9	5.5	*	-	5.0	-			
6.0	1.0	4.5	0.85	0.75	0.8	1.7	1.1	5.5	*	**	5.0	8.0			
6.0	1.0	4.5	0.65	0.55	0.8	1.4	0.9	5.5	*	-	5.0	-			
6.0	1.0	4.5	0.90	0.80	0.8	1.9	1.0	5.5	*	-	5.0	-			
6.0	1.0	4.5	0.85	0.75	0.8	1.8	1.1	5.5	*	**	5.0	7.0			
6.0	1.0	4.5	0.75	0.65	0.8	1.7	1.0	5.5	*	-	5.0	-			
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:															
I _C	I _{in}	V _R	V _{E1}	V _{E2}	V _{E3}	V _{th1}	V _{th0}	V _{out}	V _{CR}	V _{CRH}	V _{CC}	V _{CCH}	Gnd		
-	-	2,3,5,6,7,8,9,13,14	-	-	-	-	-	-	-	-	4	-	1,10		
-	-	1	-	-	-	-	-	-	-	-	4	-	2,3,5,6,7,8,9,10,13,14		
-	-	1	12	-	-	-	-	-	11	-	4	-	2,3,5,6,7,8,9,10,13,14		
-	1	-	12	-	-	-	-	-	11	-	4	-	2,3,5,6,7,8,9,10,13,14		
-	1	-	-	-	-	-	-	-	-	-	4	-	2,3,5,6,7,8,9,10,13,14		
-	-	-	-	12	-	-	1	-	11	-	4	-	2,3,5,6,7,8,9,10,13,14		
11	-	-	12	-	-	1	-	-	-	-	4	-	2,3,5,6,7,8,9,10,13,14		
-	-	-	-	-	12	-	-	11	-	-	4	-	1,2,3,5,6,7,8,9,10,13,14		
-	-	-	-	-	12	-	-	-	-	11	-	4	1,2,3,5,6,7,8,9,10,13,14		
-	-	-	-	-	12	-	-	-	-	-	4	-	10		
-	-	-	-	-	12	-	-	-	-	-	4	-	1,2,3,5,6,7,8,9,10,13,14		

* Indicated pins tied to V_{CC} thru 800 ohms ± 1.0% resistor.

** Indicated pins tied to V_{CCH} thru 800 ohms ± 1.0% resistor.

Ⓢ V_{CE} is referenced to the emitter Voltage (Pin 12).

[REDACTED]

MTTL III

INTEGRATED CIRCUITS MC3000 SERIES

[REDACTED]

MTTL III

INTEGRATED CIRCUITS

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MC3015	Single 8-Input NAND Gate	4-102
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MC3061	Dual J-K Flip-Flop	4-141
MC3062	Dual J-K Flip-Flop	4-145

NUMERICAL INDEX (Functions and Characteristics)

V_{CC} = 5.0 V, T_A = 25°C

Function	Type	Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Power Dissipation mW typ/pkg	Page No.
Quad 2-Input NAND Gate	MC3000	10	6.0	88	4-112
Quad 2-Input AND Gate	MC3001	10	9.0	112	4-110
Quad 2-Input NOR Gate	MC3002	10	6.0	122	4-114
Quad 2-Input OR Gate	MC3003	10	9.0	150	4-116
Triple 3-Input NAND Gate	MC3005	10	6.0	66	4-108
Dual 4-Input NAND Gate	MC3010	10	6.0	44	4-104
Single 8-Input NAND Gate	MC3015	10	8.0	22	4-102
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC3020	10	6.0	62.5	4-106
Dual 4-Input NAND Power Gate	MC3025	20	6.0	70	4-120
Dual 4-Input AND Power Gate	MC3026	20	9.0	90	4-118
Dual 3-Input 3-Output AND Series Terminated Line Driver	MC3028	*	9.0	56	4-124
Dual 3-Input 3-Output NAND Series Terminated Line Driver	MC3029	*	6.0	44	4-126
Dual 4-Input Expander for AND-OR-INVERT Gates	MC3030	**	***	15	4-122
AND J-K Flip-Flops	MC3050	10	f = 40 MHz	80	4-128
AND Input J \bar{J} -K \bar{K} Flip-Flop	MC3052	10	f = 40 MHz	75	4-133
Dual Type \bar{D} Flip-Flop	MC3060	10	f = 30 MHz	120	4-138
Dual J-K Flip-Flop	MC3061	10	f = 50 MHz	100	4-141
Dual J-K Flip-Flop	MC3062	10	f = 50 MHz	100	4-145

*Direct Output = 10 minus the number of resistor-terminated outputs being used.

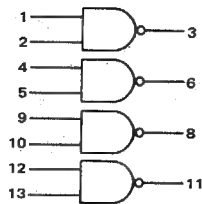
**Full output loading factor of the expandable gate is maintained.

*** Δt_{pd} = +1.0 ns typ when added to the expandable AND-OR-INVERT Gate.

$\Delta t_{pd}/pF$ = +1.0 ns pF typ caused by additional capacitance at expansion points.

GATES

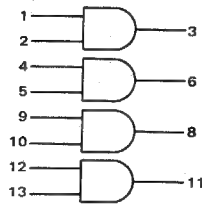
MC3000
Quad 2-Input NAND Gate



$$3 = 1 \cdot 2$$

$t_{pd} = 6.0 \text{ ns typ}$
 $P_D = 88 \text{ mW typ/pkg}$

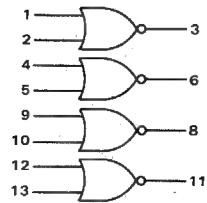
MC3001
Quad 2-Input AND Gate



$$3 = 1 \cdot 2$$

$t_{pd} = 9.0 \text{ ns typ}$
 $P_D = 112 \text{ mW typ/pkg}$

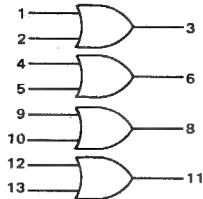
MC3002
Quad 2-Input NOR Gate



$$3 = \overline{1 + 2}$$

$t_{pd} = 6.0 \text{ ns typ}$
 $P_D = 122 \text{ mW typ/pkg}$

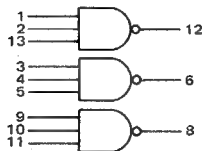
MC3003
Quad 2-Input OR Gate



$$3 = 1 + 2$$

$t_{pd} = 9.0 \text{ ns typ}$
 $P_D = 150 \text{ mW typ/pkg}$

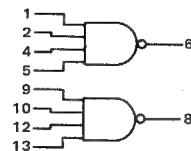
MC3005
Triple 3-Input NAND Gate



$$12 = \overline{1 \cdot 2 \cdot 13}$$

$t_{pd} = 6.0 \text{ ns typ}$
 $P_D = 66 \text{ mW typ/pkg}$

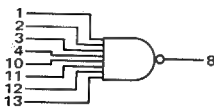
MC3010
Dual 4-Input NAND Gate



$$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$$

$t_{pd} = 6.0 \text{ ns typ}$
 $P_D = 44 \text{ mW typ/pkg}$

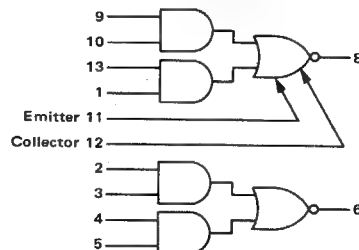
MC3015
Single 8-Input NAND Gate



$$8 = \overline{1 \cdot 2 \cdot 3 \cdot 4 \cdot 10 \cdot 11 \cdot 12 \cdot 13}$$

$t_{pd} = 8.0 \text{ ns typ}$
 $P_D = 22 \text{ mW typ/pkg}$

MC3020
Expandable Dual 2-Wide 2-Input
AND-OR-INVERT Gate



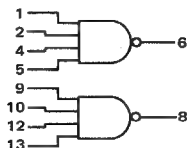
$$8 = \overline{(9 \cdot 10) + (13 \cdot 1) + (\text{Expanders})}$$

$t_{pd} = 6.0 \text{ ns typ}$
 $P_D = 62.5 \text{ mW typ/pkg}$

LOGIC DIAGRAMS (continued)

POWER GATES

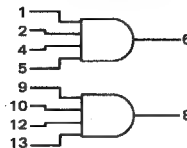
MC3025
Dual 4-Input NAND Power Gate



$$6 = 1 \cdot 2 \cdot 4 \cdot 5$$

$t_{pd} = 6.0 \text{ ns typ}$
 $P_D = 70 \text{ mW typ/pkg}$

MC3026
Dual 4-Input AND Power Gate

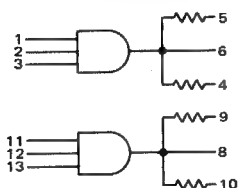


$$6 = 1 \cdot 2 \cdot 4 \cdot 5$$

$t_{pd} = 9.0 \text{ ns typ}$
 $P_D = 90 \text{ mW typ/pkg}$

LINE DRIVERS

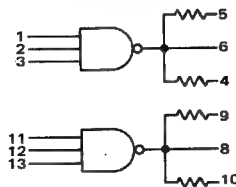
MC3028
Dual 3-Input 3-Output AND
Series Terminated Line Driver



$$4, 5, 6 = 1 \cdot 2 \cdot 3$$

$t_{pd} = 9.0 \text{ ns typ}$
 $P_D = 56 \text{ mW typ/pkg}$

MC3029
Dual 3-Input 3-Output NAND
Series Terminated Line Driver

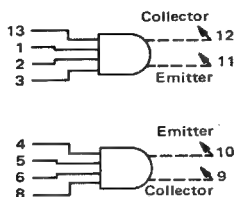


$$4, 5, 6 = 1 \cdot 2 \cdot 3$$

$t_{pd} = 6.0 \text{ ns typ}$
 $P_D = 44 \text{ mW typ/pkg}$

EXPANDER

MC3030
Dual 4-Input Expander for
AND-OR-INVERT Gates



$\Delta t_{pd} = +1.0 \text{ ns typ}$
When added to the expandable
"AND-OR-INVERT" gate.

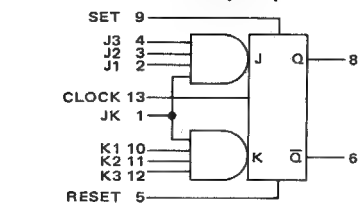
$\Delta t_{pd/pF} = +1.0 \text{ ns pF typ}$
Caused by additional capacitance
at expansion points.

$P_D = 15 \text{ mW typ/pkg}$

LOGIC DIAGRAMS (continued)

FLIP-FLOPS

**MC3050
AND J-K Flip-Flop**



J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

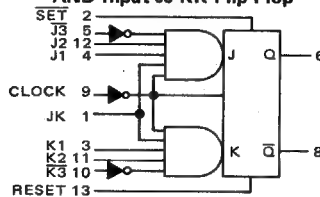
Where:

$$J = J1 \cdot J2 \cdot J3 \cdot JK$$

$$K = K1 \cdot K2 \cdot K3 \cdot JK$$

$f = 40 \text{ MHz}$
 $P_D = 80 \text{ mW typ/pkg}$

**MC3052
AND Input JJ-KK Flip-Flop**



J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

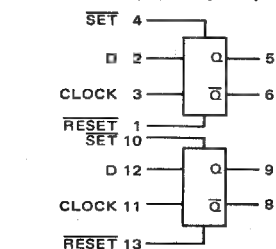
Where:

$$J = J1 \cdot J2 \cdot \bar{J3} \cdot JK$$

$$K = K1 \cdot K2 \cdot \bar{K3} \cdot JK$$

$f = 40 \text{ MHz}$
 $P_D = 75 \text{ mW typ/pkg}$

**MC3060
Dual Type D Flip-Flop**

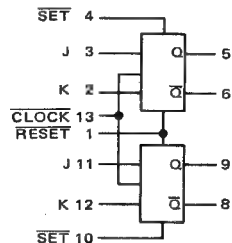


D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$$Q_{n+1} = D_n$$

$f = 30 \text{ MHz}$
 $P_D = 120 \text{ mW typ/pkg}$

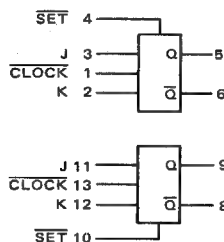
**MC3061
Dual J-K Flip-Flop**



J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$f = 50 \text{ MHz}$
 $P_D = 100 \text{ mW typ/pkg}$

**MC3062
Dual J-K Flip-Flop**



J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$f = 50 \text{ MHz}$
 $P_D = 100 \text{ mW typ/pkg}$

MTTL III

GENERAL INFORMATION SECTION

INTRODUCTION

MTTL III integrated circuits are designed with speed approaching the limit for saturated logic and for good load driving capability. This line includes all the characteristics that have made transistor-transistor logic so popular. The major advantage of MTTL III over other TTL lines is the square transfer characteristic (Figure 1) that exists only for the MTTL III family. Because of this "ideal" transfer characteristic, the MTTL III family is the only TTL line that is truly compatible with MDTL. Another advantage of this family over competitive TTL lines is that it is designed to minimize problems associated with ringing.

The circuits in the MTTL III family are distinguished by a multiple-emitter input transistor, a darlington active "pull-up" in the upper output network, and an active bypass network in the base of the output pull-down transistor as shown in Figure 2.

The multiple-emitter input configuration offers the maximum logic capability in the minimum physical area and provides improved switching characteristics during turnoff. Clamp diodes are provided at each of the inputs to limit undershoot that occurs in typical system applications such as driving long interconnect wiring. The

Darlington output configuration provides very low output impedances in each of the two output states. These low impedances result in excellent ac noise immunity and allows high-speed operation while driving large capacitive loads.

The active bypass shown in the dotted area of Figure 2 holds the phase inverter transistor "off" until gate threshold is reached. This circuit operation provides the squared transfer characteristic shown in Figure 1.

In addition to improving the transfer characteristic, the bypass network offers a number of advantages compared to a simple resistor that can be traced to a much smaller impedance variation with temperature.

1. Lower bypass impedance for the reverse current of the output transistor at elevated temperatures, provides faster turn-off.
2. A lower current spike during the turn-off transient causes a lower ac power factor resulting in a lower total power consumption. This advantage is even more pronounced at higher temperatures.
3. Faster turn-on at low temperature.

FIGURE 1 — COMPARISON OF CONVENTIONAL TRANSISTOR-TRANSISTOR LOGIC AND MTTL III

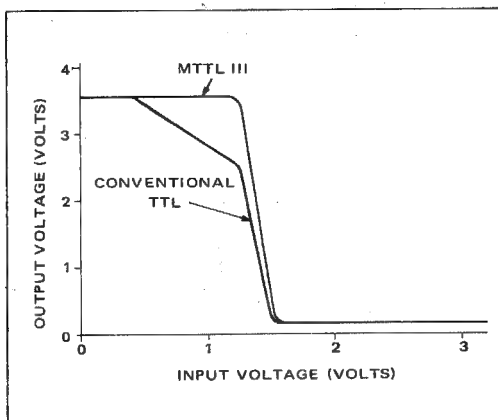
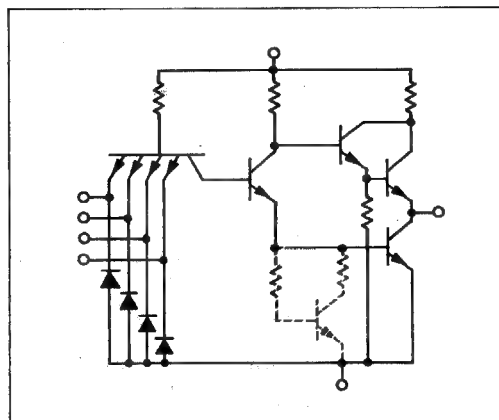


FIGURE 2 — TYPICAL MTTL III CIRCUIT



TYPICAL CHARACTERISTICS

Typical operating characteristics of the MTTL III family include: (Unless otherwise indicated, the parameters are defined for $V_{CC} = +5.0$ volts and $T_A = +25^\circ\text{C}$.)

Supply Voltage Operating Range = 4.5 to 5.5 volts

Operating Temperature Range: MC3000 Series
0 to $+75^\circ\text{C}$

Output Drive Capability

Gates (Output Loading Factor):
MC3000 Series = 10 Gates

Capacitance = 600 pF

Output Impedance

High State = 10 ohms nominal (unsaturated)
Low State = 10 ohms nominal

Output Voltage Swing = 0.2 to 3.5 volts typical

Input Voltage Limits

+5.5 volts maximum
-1.5 volts minimum (1)

Switching Threshold = 1.5 volts nominal

Input Impedance

High State = 400 k ohms nominal
Low State = 2.4 k ohms nominal

Worst-Case dc Noise Margin

High State = 0.700 volt minimum
Low State = 0.700 volt minimum

Power Dissipation

22 mW per gate typical
50-80 mW per flip-flop typical

Switching Speeds (2)

Average Propagation Delay = 6.0 ns per gate typical
13 ns per flip-flop typical

Rise Time = 1.0 ns typical

Fall Time = 1.3 ns typical

Flip-Flop Clock Frequency (MC3064) = 50 MHz maximum.

"NAND" GATES

The basic gate of the MTTL III logic family is the positive logic NAND gate. This gate is characterized by high speed, good load driving capability, superior transfer characteristic, and freedom from ringing problems. Representative of the various NAND gates presently available in the MTTL III family is the 4-input NAND gate (1/4 of the MC3010) shown in Figure 3.

"AND" GATES

While it is possible to design a complete logic system with NAND logic, it is often desirable to use other logic forms to save circuits, power dissipation, and propagation delay. Therefore, the positive logic AND function has been added to the MTTL III family.

Examples of the AND function are the standard quad 2-input gate, dual 4-input gate, dual 4-input power gate and a dual 3-input, 3-output line driver.

The technique used to form the AND function is the addition of an inverter to the basic NAND circuit. As shown in Figure 4, the inverter transistor with a collector resistor and an offset diode connected to its emitter is inserted between the multiple-emitter input transistor and the basic circuit phase-splitter transistor. The extra inversion adds only 3.0 ns propagation delay and about 6.0 mW additional power dissipation.

FIGURE 3 – MTTL III POSITIVE LOGIC "NAND" GATE CIRCUIT

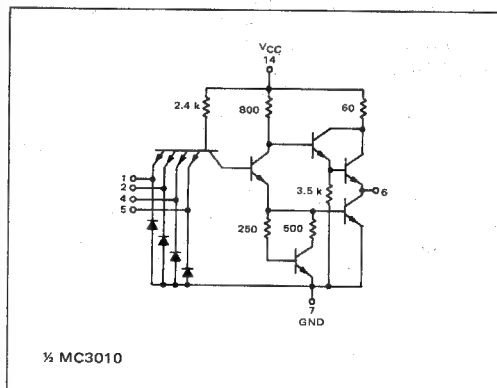
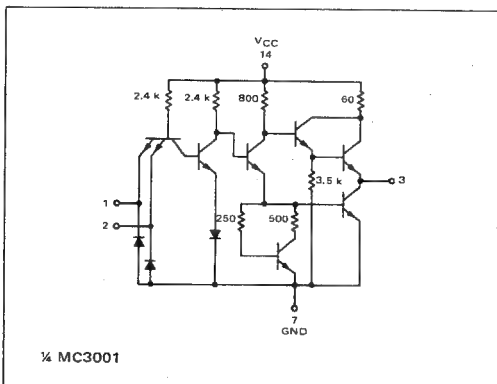


FIGURE 4 – MTTL III POSITIVE LOGIC "AND" GATE CIRCUIT



(1) Assuming unused inputs are returned to voltage not greater than 4.0 Vdc.

(2) The switching characteristics of the MTTL III family are defined with respect to the associated transitions of the voltage waveforms. The average propagation delay is defined as the average of the turn-on delay and the turn-off delay measured from the 1.5 V point of the input to the 1.5 V point of the associated output transition or:

$$t_{pd} = \frac{t_{on} + t_{off}}{2} \text{ ns}$$

Rise time is defined as the positive going transition of the output from the 1.0 V to the 2.0 V level. Fall time is defined as the negative output transition from the 2.0 V to the 1.0 V level.

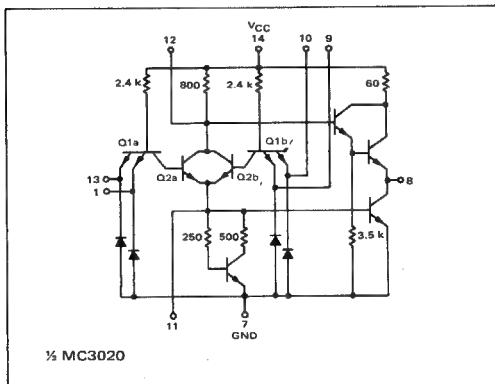
"AND-OR-INVERT" GATES

Unlike the MDTL family of logic circuits, the outputs of MTTL logic circuits cannot be tied together to perform the "Implied AND", often called the "Wired OR" function. If the outputs of the MTTL family devices are tied together, the lower output transistor of one circuit and the upper output transistor of another circuit can be "on" simultaneously. This condition provides a low-impedance path from V_{CC} to ground, and due to excessive current flow, the saturated output state cannot be maintained and the desired logic function is not satisfied.

To retain the logical advantages offered by the "Implied AND" with the speed and load driving capability of an active pull-up, the MTTL III family offers an AND-OR-INVERT Gate. The gate in Figure 5 incorporates two 2-input AND functions with outputs that are ORed and inverted. The AND function is provided by two multiple-emitter input transistors (Q1a and Q1b). The OR and INVERT operation is accomplished by two paralleled transistors (Q2a and Q2b) sharing a single collector resistor and a single bypass network. These paralleled transistors in turn drive the standard output.

The common collector and emitter nodes of one gate in each package are available externally to permit expansion.

FIGURE 5 — MTTL III "AND-OR-INVERT" GATE CIRCUIT



EXPANDER AND EXPANDER NODES

The ORing nodes of 1/2 the MC3020 dual AND-OR-INVERT Gate (Figure 5) are available for expanding the number of AND gates to four. Since these are comparatively high-impedance nodes, care should be taken to minimize capacitive loading on the expander terminals if switching speed is to be maintained. When an expander is to be used with an expandable AND-OR-INVERT gate, it should be placed as close as possible to the gate being expanded. The increase in the average propagation delay per AND gate added to an expandable AND-OR-INVERT gate is typically 1.0 ns/AND gate. The increase in average propagation delay as a function of capacitance added to the expander nodes is typically 1.0 ns/pF.

"NOR" GATES

To save inverters, the system designer often needs the positive logic NOR function as well as the negative logic NOR available with the standard NAND gate. This capability is incorporated in the MTTL III line in the form of the MC3002, quad 2-input NOR Gate. The NOR gate is a modified AND-OR-INVERT gate with only a single emitter on each input transistor, as shown in Figure 6.

"OR" GATES

To provide the system designer with still another tool for optimum design, the MTTL III Series also offers the positive logic OR function. As shown in Figure 7, the OR is essentially a NOR gate with an additional inverter.

POWER GATES

Standard MTTL III gates offer good load driving capability and high fan-out. In most systems, however, there are a few applications that exceed the capability of a standard gate. The MTTL III power gates, shown in Figure 8, are designed to meet these requirements with a minimum of additional circuitry. Available in both NAND and AND functions, the power gates feature output circuitry designed to provide twice the fan-out of conventional gates: 20 standard gate loads instead of 10.

FIGURE 6 — MTTL III POSITIVE LOGIC "NOR" GATE CIRCUIT

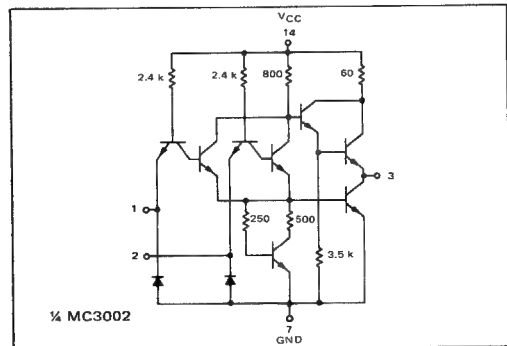
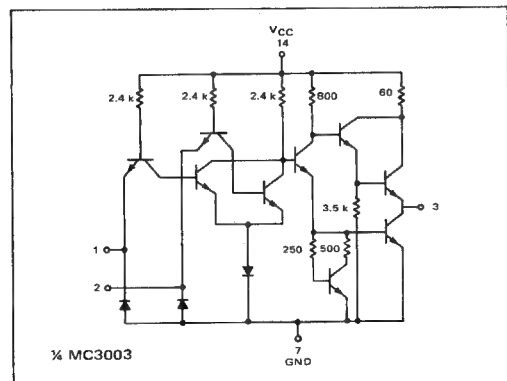


FIGURE 7 — MTTL III POSITIVE LOGIC "OR" GATE CIRCUIT



LINE DRIVERS

To minimize switching transients on long lines, the MTTL III family includes dual 3-input/3-output series-terminated line drivers. Two outputs have 75-ohm resistors in series with the standard output node, and one is connected directly to the node. A good match can be made at the output of each resistor when driving 93-ohm coax or 120-ohm twisted pair. For loads of 50 to 93 ohms, the two resistive outputs are paralleled for impedance matching. The non-resistive output can be used to drive adjacent loads in a normal fashion. The total number of output loads connected to the direct output (non-resistive output) is the standard fan-out of 10, minus the number of resistor terminated outputs being used.

Figure 9 shows 1/2 of the circuit of the MC3029, dual 3-input, 3-output series terminated NAND line driver. Figure 10 shows a typical application of this circuit and Figure 11 demonstrates the effects of series termination without a significant loss in high state noise immunity.

FIGURE 8 – MTTL III POWER GATE CIRCUIT (AND)

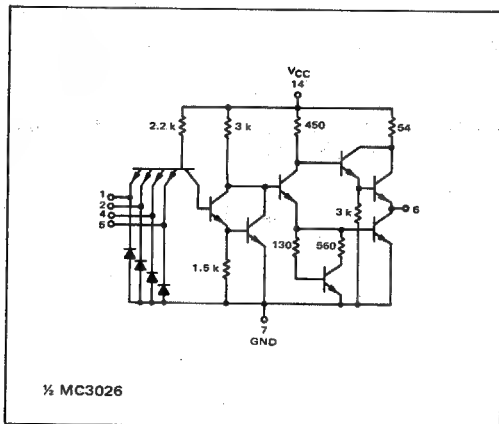
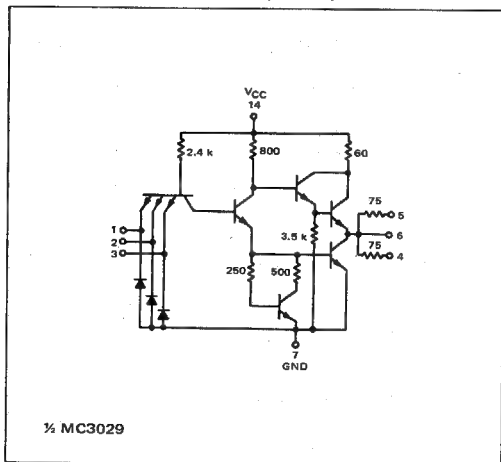


FIGURE 9 – MTTL III TERMINATED LINE DRIVER (NAND)



MTTL III

GENERAL INFORMATION
SECTION

FIGURE 10 – TYPICAL APPLICATION OF THE LINE DRIVER

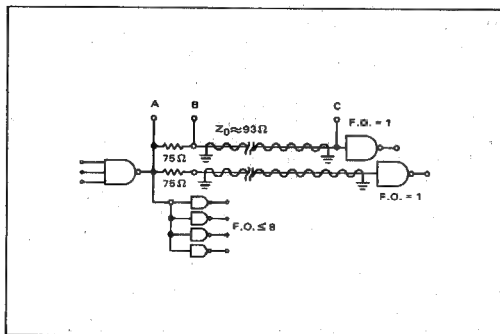
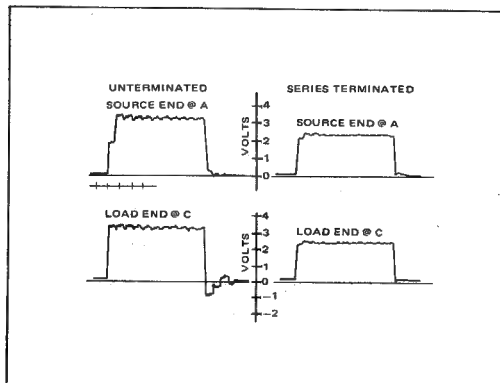


FIGURE 11 – EFFECTS OF SERIES TERMINATION WITH A MTTL III GATE DRIVING A 93-OHM LINE



OPERATING CHARACTERISTICS OF FLIP-FLOPS

The cornerstone of any modern logic family is the capability of its storage elements. The MTTL III flip-flops are designed to give maximum logic performance with fewer system restrictions than their predecessors. Three basic designs are typified by the MC3050, MC3060 and MC3061/MC3062. Common to all designs are:

1. Edge clocking.

The flip-flop is clocked at the normal MTTL III threshold voltage (approximately 1.5 V @ 25°C).

2. Overriding asynchronous inputs.

The direct SET and RESET inputs control the operation of the flip-flop regardless of the state of the clock or the information on synchronous inputs.

3. Short set-up times.

Prior to the clocking edge, the input information must become stable. The MTTL III flip-flops require only a minimum of time to read a "1" or a "0". Therefore data may be applied anytime in the clock period except during the time interval between the Set-up and Hold times. This characteristic permits higher clock frequencies or eliminates the necessity for critical control of clock pulse width.

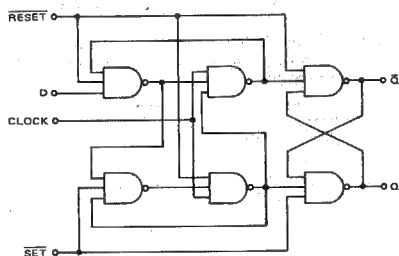
4. All inputs to the storage elements including the clock input have inputs that are compatible with all three MTTL families.

The MC3050 and MC3060 flip-flops are positive edge triggered storage elements. That is, the inputs are enabled on the negative edge of the clock and the information is stored in the flip-flop on the positive edge of the clock. The MC3061 and MC3062 dual flip-flops are negative edge triggered devices and therefore operate in precisely the opposite manner. That is, data is stored on the negative edge of the clock.

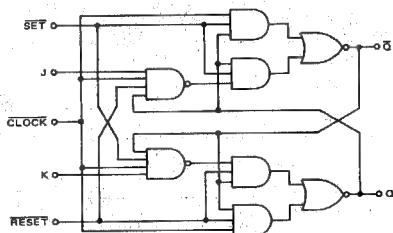
In addition to the previously mentioned storage elements, The MC3052 Master-Slave flip-flop is also available. Data is stored in the Master flip-flop when the clock is low and transferred to the Slave flip-flop when the clock goes high.

Detailed discussion of each of the MTTL III flip-flops is provided on the individual data sheets.

FIGURE 12 — LOGIC DIAGRAMS OF EDGE-CLOCKED
MTTL III FLIP-FLOPS

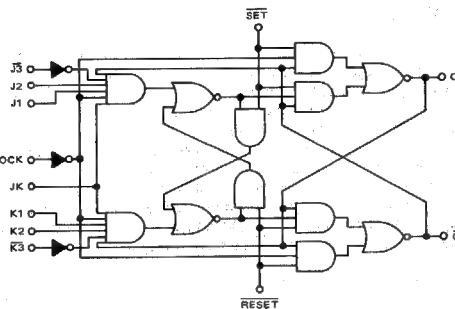


MC3060

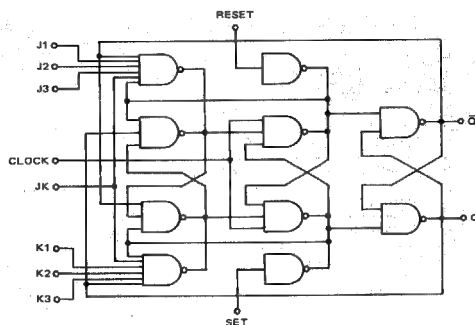


MC3061

FIGURE 13 — LOGIC DIAGRAM OF MTTL III
MASTER-SLAVE J-K FLIP-FLOP



MC3052



MC3050

BREADBOARDING SUGGESTIONS

When breadboarding with any form of high-speed, high-performance TTL circuit, the designer must always be aware of the problems caused by very high switching speeds. These switching speeds, especially the frequencies associated with the very fast rise and fall times of the circuits, are in the upper RF range and good high-frequency layout techniques should be used. The following breadboarding suggestions will help the designer in his initial circuit layout. In many cases the breadboarding suggestions will have to be modified to meet the requirements of the designer's specific application.

Power and Ground Distribution

Special care should be taken to insure adequate distribution of power and ground systems. The typical rates of change of current and voltage for a single MTTL III gate are in the range of 10^7 A/s and 10^8 V/s respectively. These figures reflect the necessity for a low-impedance power supply and ground distribution system, if transients are to be minimized and noise margins maintained. The use of AWG No. 20 wire or larger is often required. For printed circuitry, line widths of 100 mils or more are often necessary. A ground plane is desirable when using a large number of units.

Bypassing

To reduce supply transients, the breadboard should be bypassed at the point where power is supplied to the board and at intervals throughout the board. The use of a single bypass capacitor at the output terminal of the power supply is not adequate in a breadboard utilizing the fast rise and fall time MTTL III circuits. A comparatively large, low-inductance type capacitor (in the $1.0 \mu\text{F}$ range) is suggested at the point where power and ground enter the board. In many cases it has been found that distributing $0.01 \mu\text{F}$ capacitors for every five packages throughout a breadboard is adequate to suppress normal switching transients. It is also suggested that a bypass capacitor be placed in close proximity to any circuit driving a large capacitive load.

Power Dissipation

The typical average dc power dissipation is given for each MTTL III device (3). It should be noted that the totem-pole output common to all high-level MTTL circuits has an associated ac power dissipation factor. This factor results from the timing overlap of the upper and lower output transistors during the normal switching operation and is typically $0.4 \text{ mW/MHz/output}$ for a 15-pF load. This ac power dissipation should be added when calculating the total power requirements of the MTTL III circuits.

Unused Inputs and Unused Gates

To minimize potential problems resulting from external noise, the unused inputs of any MTTL III logic circuit should not be left open, but should either be tied to the used inputs or returned to a voltage between 2.0 and 5.5 Vdc. (For flip-flops, see appropriate data sheet for additional detail.) If the unused inputs are returned to a voltage, care should be exercised to insure that the absolute voltage between the most negative input level and that voltage does not exceed +5.5 volts. The total number of inputs that can be tied to the output of any driving gate is 25. (This is defined as high-state output loading factor.) It should be noted that the low-state output loading rules must still be maintained. The minimum logical "1" level for the high-state output loading is summarized for $V_{CC} = 5.0 \text{ V}$, $V_{IL} = 1.1 \text{ V}$, and $I_{OH} = -2.0 \text{ mA}$: $V_{OH} = 2.5$ volts minimum @ 0°C .

To minimize power drain, the inputs of any unused gate in a package should be maintained at the level that would place the outputs in the high state (the low power dissipation state).

$$(3) P_D = \frac{I_{PDL} + I_{PDH}}{2} (V_{CC})$$

where I_{PDL} and I_{PDH} are the typical current drains at $V_{CC} = +5.0 \text{ V}$.

MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage — Continuous	+7.0	Vdc
Supply Operating Voltage Range	4.5 to 5.5	Vdc
Input Voltage	+5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range	0 to +75	$^\circ\text{C}$
Storage Temperature Range — Flat Package	-65 to +175	$^\circ\text{C}$
Plastic Package	-55 to +125	$^\circ\text{C}$

MTTL III

GENERAL INFORMATION SECTION

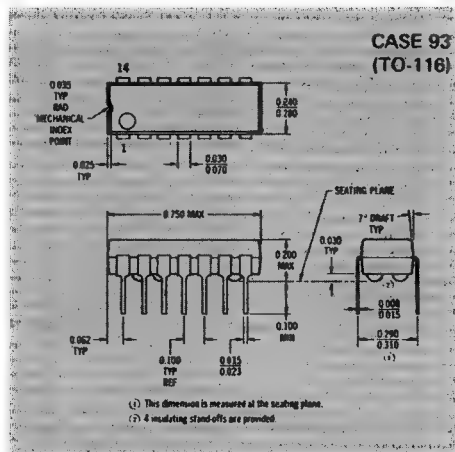
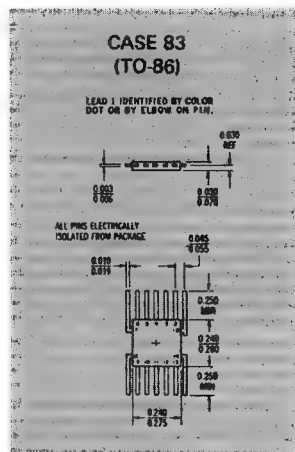
DEFINITIONS

BV_{in}	Input breakdown voltage
C_T	Total parasitic capacitance, which includes probe, wiring, and load capacitances
I_C	Collector current
I_{CO}	Expander collector leakage current
I_D	Input diode current with negative voltage applied
I_E	Emitter current
I_{EO}	Expander emitter leakage current
I_{EXE}	Expander drive current at emitter node of AND-OR-INVERT gate
I_F	Input forward current with V_{CC} applied
I_{F1}	Input forward current with V_{CC} applied
I_{F2}	Input forward current with V_{CC} applied
I_{FC}	Clock input forward current
I_{FD}	D input forward current
I_{FJ}	J input forward current
I_{FK}	K input forward current
I_{FJK}	JK input forward current
I_{FR}	RESET input forward current
I_{FS}	SET input forward current
I_{in}	Input current
I_{max}	Maximum rated power supply current with V_{max} applied
I_{OH}	Output high state current
I_{OHA}	Unterminated output high state current
$I_{OHS, C}$	Terminated output high state current
I_{OL}	Output low state current
I_{OL1}	Output low state current with V_{CC} applied
I_{OL1A}	Unterminated output low state current with V_{CC} applied
I_{OL2}	Output low state current with V_{CC} applied
I_{OL2A}	Unterminated output low state current with V_{CC} applied
$I_{OL1B, 1C}$	Terminated output low state current with V_{CC} applied
$I_{OL2A, 2C}$	Terminated output low state current with V_{CC} applied
I_{PD}	Flip-flop power supply drain current
I_{PDH}	Power supply drain with inputs high
I_{PDL}	Power supply drain with inputs low
I_R	Input leakage current
I_{RC}	Clock input leakage current
I_{RD}	D input leakage current
I_{RJ}	J input leakage current
I_{RK}	K input leakage current

I_{RJK}	JK input leakage current
I_{RR}	RESET input leakage current
I_{RS}	SET input leakage current
I_{SC}	Short-circuit current
P_1	Pulse used to set flip-flop state
PRF	Pulse repetition frequency
PW	Pulse width
t_f	Fall time
$t_{Hold "0"}$	Minimum time that low state data must be maintained after the clocking edge
$t_{Hold "1"}$	Minimum time that high state data must be maintained after the clocking edge
Δt_{pd}	Average increase in propagation delay per expander AND gate when connected to an AND-OR-INVERT gate
$\Delta t_{pd}/PF$	Increased propagation delay caused by additional capacitance at expansion points
$t_{pd} "0"$	Turn-on delay
$t_{pd} "1"$	Turn-off delay
t_r	Rise time
$t_{sd} "0"$	Turn-on delay from asynchronous input
$t_{sd} "1"$	Turn-off delay from asynchronous input
$t_{Set "0"}$	Minimum time that high state data must be applied prior to the clocking edge
$t_{Set "1"}$	Minimum time that high state data must be applied prior to the clocking edge
TP_{in}	Test point at input of device under test
TP_{out}	Test point at output of device under test
$V_{BE max}$	Emitter node threshold voltage for logic "0" output level
$V_{BE min}$	Emitter node threshold voltage for logic "1" output level
V_{CC}	Power supply voltage
V_{CCH}	High power supply voltage
V_{CCL}	Low power supply voltage
V_D	Diode clamp voltage
V_{EE1}	Voltage applied to expander emitter for V_{OL} test
V_{EE2}	Voltage applied to expander emitter node for I_{CO} test
V_F	Maximum logic "0" level output voltage
V_{IH}	Logic "1" threshold voltage
V_{IHx}	Reduced supply voltage to hold input above threshold and to prevent noise from entering the device
V_{IL}	Logic "0" threshold voltage
V_{max}	Maximum rated power supply voltage
V_{OH}	Output high voltage with I_{OH} source current
V_{OL}	Output low voltage with I_{OL} source current
V_{OL1}	Maximum output low voltage with V_{CC} applied
V_{OL2}	Maximum output low voltage with V_{CCH} applied
V_{OL3}	Maximum output low voltage on terminated output with V_{CCL} applied
V_{OL4}	Maximum output low voltage on terminated output with V_{CCH} applied
V_R	Logic "1" minimum reverse voltage
V_{RH}	Logic "1" maximum reverse voltage

PACKAGING

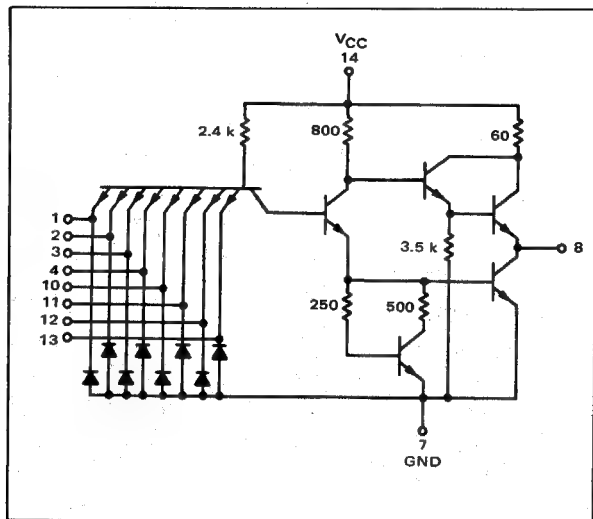
All MTTL III integrated circuits are available in the TO-85 14 lead flat package and TO-116 dual in-line plastic package. Suffix "F" to the basic type number; to order plastic package, add Suffix "P".



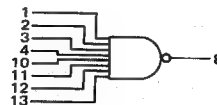
SINGLE 8-INPUT "NAND" GATE

MTTL III MC3000 series

MC3015



This device is an 8-input NAND gate. It is useful when processing a large number of variables, such as in encoders and decoders.



Positive Logic:

$$8 = 1 \cdot 2 \cdot 3 \cdot 4 \cdot 10 \cdot 11 \cdot 12 \cdot 13$$

Negative Logic:

$$8 = 1 + 2 + 3 + 4 + 10 + 11 + 12 + 13$$

Input Loading Factor = 1

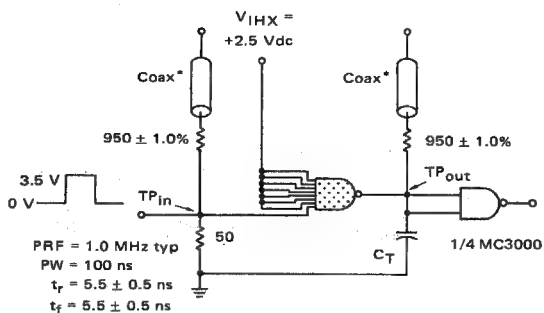
Output Loading Factor = 10

Total Power Dissipation = 22 mW typ/pkg

Propagation Delay Time = 8.0 ns typ

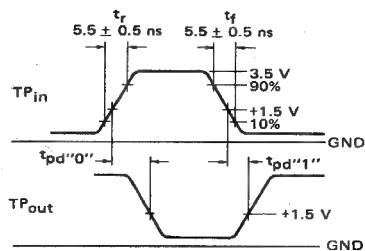
SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



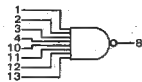
*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of this device. To complete testing, sequence through remaining inputs in the same manner.



@Test
Temperature

0°C

+25°C

+75°C

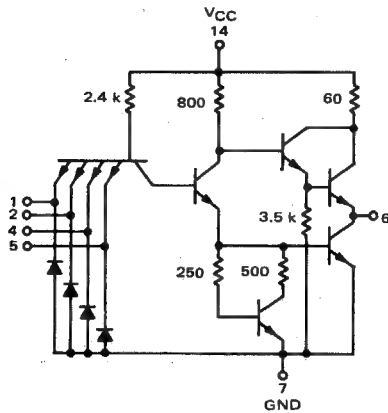
Characteristic	Symbol	Pin Under Test	MC3015 Test Limits						Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																Gnd
			0°C		+25°C		+75°C			I _{OL1}	I _{OL2}	I _{OH}	I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	V _{IHX}		
			Min	Max	Min	Max	Min	Max																		
Input																										
Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	1	-	2, 3, 4, 10, 11, 12, 13	-	-	14	-	-	-	7	
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	1	-	2, 3, 4, 10, 11, 12, 13	-	-	-	14	-	-	7	
Leakage Current	I _R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	1	-	-	-	-	-	14	-	2, 3, 4, 7, 10, 11, 12, 13		
Breakdown Voltage	BV _{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	14	-	2, 3, 4, 7, 10, 11, 12, 13		
Clamp Voltage	V _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7	
Output																										
Output Voltage	V _{OL1}	8	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	-	1	-	2, 3, 4, 10, 11, 12, 13	-	-	14	-	-	7		
	V _{OL2}	8	-	0.4	-	0.4	-	0.4	Vdc	-	8	-	-	-	-	1	-	2, 3, 4, 10, 11, 12, 13	-	-	-	14	-	-	7	
	V _{OH}	8	2.5	-	2.5	-	2.5	-	Vdc	-	-	8	-	-	1	-	-	2, 3, 4, 10, 11, 12, 13	-	-	14	-	-	7		
Short-Circuit Current	I _{SC}	8	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 3, 4, 7, 8, 10, 11, 12, 13		
Power Requirements (Total Device)																								1, 2, 3, 4, 7, 10, 11, 12, 13		
Maximum Power Supply Current	I _{max}	14	-	-	-	6.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	-	-		
Power Supply Drain	I _{PDH}	14	-	9.0	-	9.0	-	9.0	mAdc	-	-	-	-	-	-	-	-	1, 2, 3, 4, 10, 11, 12, 13	-	14	-	-	-	7		
	I _{PDL}	14	-	4.3	-	4.3	-	4.3	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 3, 4, 7, 10, 11, 12, 13		
Switching Parameters										Pulse In	Pulse Out															
Turn-On Delay	t _{pd"0"}	1, 8	-	-	-	12	-	-	ns	1	8	-	-	-	-	-	-	-	-	14	-	-	2, 3, 4, 10, 11, 12, 13	7		
Turn-Off Delay	t _{pd"1"}	1, 8	-	-	-	12	-	-	ns	1	8	-	-	-	-	-	-	-	-	14	-	-	2, 3, 4, 10, 11, 12, 13	7		

DUAL 4-INPUT "NAND" GATE

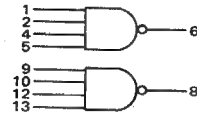
MTTL III MC3000 series

MC3010

1/2 OF CIRCUIT SHOWN



This device consists of two 4-input NAND gates. These gates may be cross-coupled to form a set-reset flip-flop.



$$\text{Positive Logic: } 6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$$

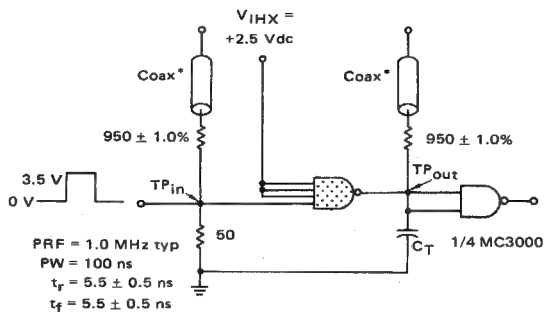
$$\text{Negative Logic: } 6 = \overline{1 + 2 + 4 + 5}$$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 44 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

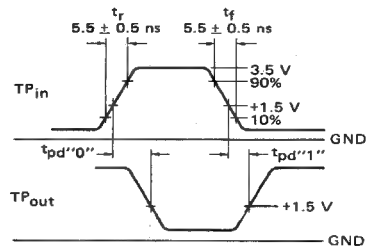
SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

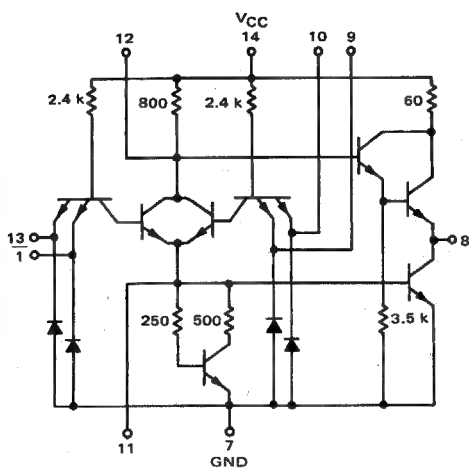


EXPANDABLE DUAL 2-WIDE 2-INPUT "AND-OR-INVERT" GATE

MC3020

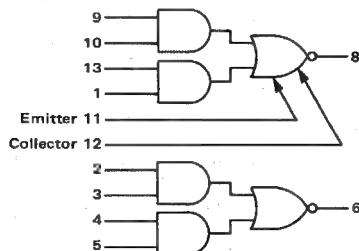
MTTL III MC3000 series

1/2 OF CIRCUIT SHOWN †



†Other half of circuit omits expander inputs.

One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together, driving an output inverter, and the ORing nodes are available for expansion. Up to four AND gates can be ORed together using the MC3030 expander. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

$$8 = (9 \cdot 10) + (13 \cdot 1) + (\text{Expanders})$$

Negative Logic:

$$8 = (9 + 10) \cdot (13 + 1) \cdot (\text{Expanders})$$

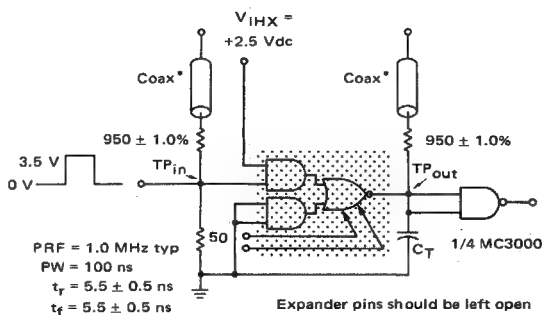
Input Loading Factor = 1

Output Loading Factor = 10

Total Power Dissipation = 62.5 mW typ/pkg

Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT

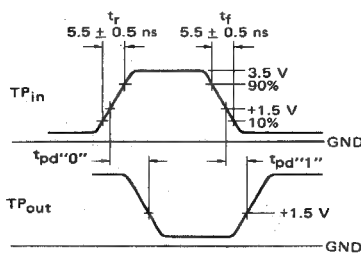


Expander pins should be left open when measuring switching times.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

@Test
Temperature

0°C

+25°C

+75°C

ELECTRICAL CHARACTERISTICS										TEST CURRENT / VOLTAGE VALUES																Gnd	
<div>Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.</div> <div>@Test Temperature 0°C +25°C +75°C</div>										mA								Volts									
										I _{OL1}	I _{OL2}	I _{OH}	I _{in}	I _D	I _E	I _{EXE}	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}		V _{IHX}
										19	23	-2.0	-	-	0.3	0.50	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5		-
										19	23	-2.0	1.0	-10	0.3	0.55	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5		2.5
										19	23	-2.0	-	-	0.3	0.70	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5		-
MC3020 Test Limits										TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																	
Characteristic	Symbol	Pin Under Test	0°C		+25°C		+75°C		Unit	I _{OL1}	I _{OL2}	I _{OH}	I _{in}	I _D	I _E	I _{EXE}	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	V _{IHX}	
			Min	Max	Min	Max	Min	Max																			
Input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	-	-	-	1	-	13	-	-	14	-	-	7, 9, 10 *
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	-	-	-	1	-	13	-	-	-	14	-	7, 9, 10 *
Leakage Current	I _R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	7, 9, 10, 13 *
Breakdown Voltage	BV _{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	14	-	7, 9, 10, 13 *
Clamp Voltage	V _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	-	-	-	14	-	-	7, 9, 10 *
Output Output Voltage	V _{OL1}	8	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	-	-	-	1	-	-	13	-	-	14	-	-	7, 9, 10 *
	V _{OL1}	8	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	-	11, 12	-	-	-	-	-	-	-	14	-	-	1, 7, 9, 10, 13
	V _{OL2}	8	-	0.4	-	0.4	-	0.4	Vdc	-	8	-	-	-	-	11, 12	-	-	-	-	-	-	-	-	14	-	1, 7, 9, 10, 13 *
	V _{OL2}	8	-	0.4	-	0.4	-	0.4	Vdc	-	8	-	-	-	-	-	-	1	-	-	13	-	-	-	14	-	7, 9, 10 *
	V _{OH}	8	2.5	-	2.5	-	2.5	-	Vdc	-	-	8	-	-	-	-	1	-	-	-	13	-	-	14	-	-	1, 7, 10 *
Short-Circuit Current	I _{SC}	8	-	-	-30	-100	-	-	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 7, 8, 9, 10, 13 *
Base-Emitter Voltage	V _{BE max}	11	-	1.010	-	0.975	-	0.935	Vdc	8	-	-	-	-	-	11, 12	-	-	-	-	-	-	-	14	-	-	1, 9, 10, 13 *
	V _{BE min}	11	0.70	-	0.65	-	0.55	-	Vdc	-	-	-	-	-	11	-	-	-	-	-	-	-	-	14	-	-	1, 9, 10, 12, 13 *
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	24	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 3, 4, 5, 7, 9, 10, 13
Power Supply Drain	I _{PDH}	14	-	22	-	22	-	22	mAdc	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 4, 5, 9, 10, 13	-	14	-	-	-	7
	I _{PDL}	14	-	14	-	14	-	14	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 3, 4, 5, 7, 9, 10, 13
Switching Parameters	Turn-On Delay t _{pd"0"}	1, 8	-	-	-	12	-	-	ns	Pulse In	Pulse Out	-	-	-	-	-	-	-	-	-	-	-	14	-	-	13	7, 9, 10 *
										1	8																
Turn-Off Delay	t _{pd"1"}	1, 8	-	-	-	12	-	-	ns	1	8	-	-	-	-	-	-	-	-	-	-	-	14	-	-	13	7, 9, 10 *

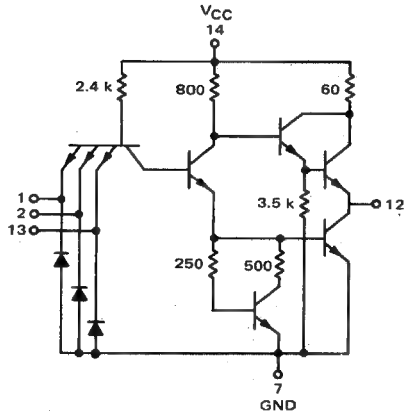
*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

TRIPLE 3-INPUT "NAND" GATE

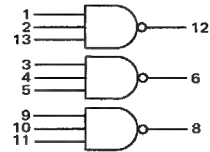
MTTL III MC3000 series

MC3005

1/3 OF CIRCUIT SHOWN



This package consists of three 3-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.



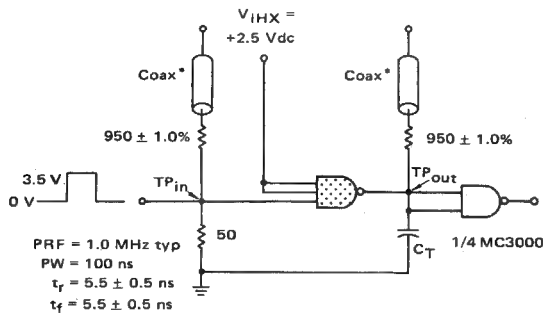
Positive Logic: $12 = \overline{1 \cdot 2 \cdot 13}$
Negative Logic: $12 = \overline{1 + 2 + 13}$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 66 mW typ /pkg
Propagation Delay Time = 6.0 ns typ

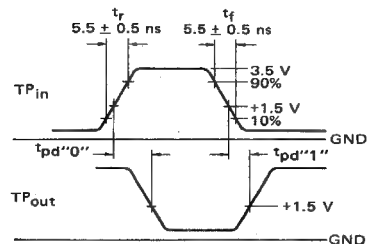
SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

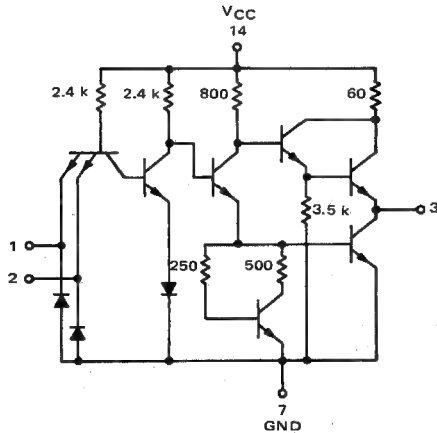


QUAD 2-INPUT "AND" GATE

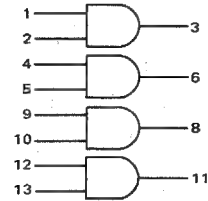
MTTL III MC3000 series

MC3001

1/4 OF CIRCUIT SHOWN



This device consists of four 2-input AND gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.



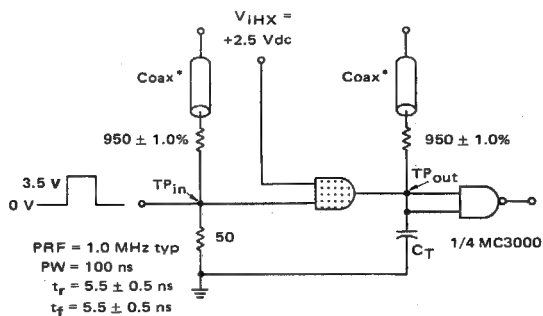
Positive Logic: $3 = 1 \cdot 2$
Negative Logic: $3 = 1 + 2$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 112 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

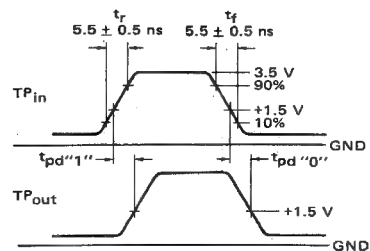
SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



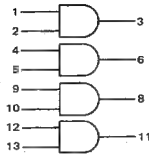
*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@Test
Temperature
0°C
+25°C
+75°C

TEST CURRENT / VOLTAGE VALUES																
mA					Volts											
I _{OL1}	I _{OL2}	I _{OH}	I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	V _{IHX}		
19	23	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5	-		
19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5	2.5		
19	23	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	-		
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																
I _{OL1}	I _{OL2}	I _{OH}	I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	V _{IHX}	Gnd	
-	-	-	-	-	-	-	1	-	2*	-	-	14	-	-	7	
-	-	-	-	-	-	-	1	-	2*	-	-	-	14	-	7	
-	-	-	-	-	-	-	-	1	*	-	-	-	14	-	2,7	
-	-	-	1	-	-	-	-	-	*	-	-	-	14	-	2,7	
-	-	-	-	1	-	-	-	-	*	-	-	14	-	-	7	
3	-	-	-	-	1	-	-	-	2*	-	-	14	-	-	7	
-	3	-	-	-	1	-	-	-	2*	-	-	-	14	-	7	
-	-	3	-	-	-	1	-	-	2*	-	-	14	-	-	7	
-	-	-	-	-	-	-	-	-	1,2*	-	14	-	-	-	3,7	
-	-	-	-	-	-	-	-	-	1,2,4,5,9,10,12,13	14	-	-	-	-	7	
-	-	-	-	-	-	-	-	-	1,2,4,5,9,10,12,13	-	14	-	-	-	7	
-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,4,5,7,9,10,12,13	
Pulse In	Pulse Out															
1	3	-	-	-	-	-	-	-	*	-	14	-	-	2	7	
1	3	-	-	-	-	-	-	-	*	-	14	-	-	2	7	

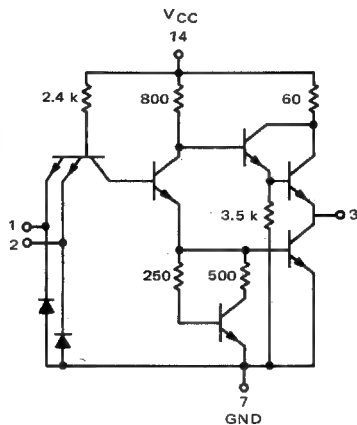
*Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH}.

QUAD 2-INPUT "NAND" GATE

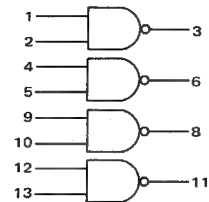
MTTL III MC3000 series

MC3000

1/4 OF CIRCUIT SHOWN



This device consists of four 2-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.

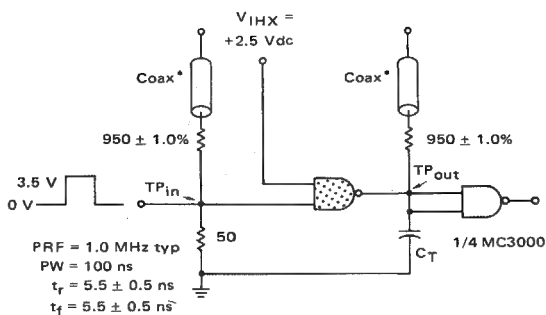


Positive Logic: $3 = \overline{1 \cdot 2}$
Negative Logic: $3 = \overline{1 + 2}$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 88 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

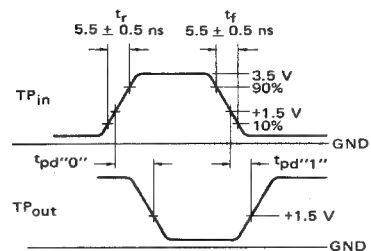
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

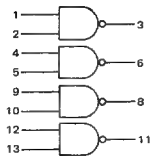
$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@Test
Temperature
0°C
+25°C
+75°C

Characteristic	Symbol	Pin Under Test	MC3000 Test Limits							Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:															Gnd
			0°C		+25°C		+75°C																			
			Min	Max	Min	Max	Min	Max	I _{OL1}		I _{OL2}	I _{OH}	I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	V _{IHX}		
Input																										
Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	1	-	2	-	-	14	-	-	7 *		
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	1	-	2	-	-	-	14	-	7 *		
Leakage Current	I _R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2,7 *		
Breakdown Voltage	BV _{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	14	-	2,7 *		
Clamp Voltage	V _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	14	-	-	7 *		
Output																										
Output Voltage	V _{OL1}	3	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	-	-	1	-	-	2	-	-	14	-	-	7 *	
	V _{OL2}	3	-	0.4	-	0.4	-	0.4	Vdc	-	3	-	-	-	-	1	-	-	2	-	-	-	14	-	7 *	
	V _{OH}	3	2.5	-	2.5	-	2.5	-	Vdc	-	-	3	-	-	1	-	-	-	2	-	-	14	-	-	7 *	
Short-Circuit Current	I _{SC}	3	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 3, 7 *	
Power Requirements (Total Device)																										
Maximum Power Supply Current	I _{max}	14	-	-	-	25	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13	
Power Supply Drain	I _{PDH}	14	-	36	-	36	-	36	mAdc	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	-	-	7	
	I _{PDL}	14	-	17.5	-	17.5	-	17.5	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13	
Switching Parameters										Pulse In	Pulse Out															
Turn-On Delay	t _{pd"0"}	1, 3	-	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	-	-	14	-	-	2	7 *		
Turn-Off Delay	t _{pd"1"}	1, 3	-	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	-	-	14	-	-	2	7 *		

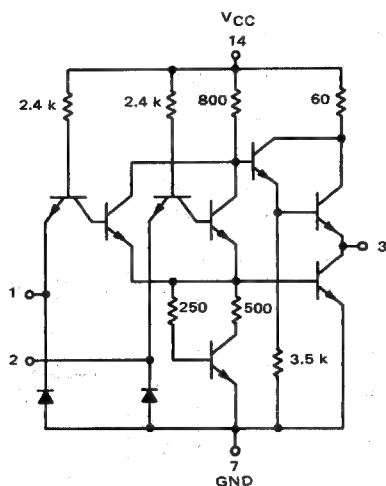
* Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

QUAD 2-INPUT "NOR" GATE

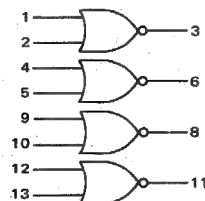
MTTL III MC3000 series

MC3002

1/4 OF CIRCUIT SHOWN



This device consists of four 2-input NOR gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.



Positive Logic: $3 = \overline{1+2}$

Negative Logic: $3 = \overline{1 \cdot 2}$

Input Loading Factor = 1

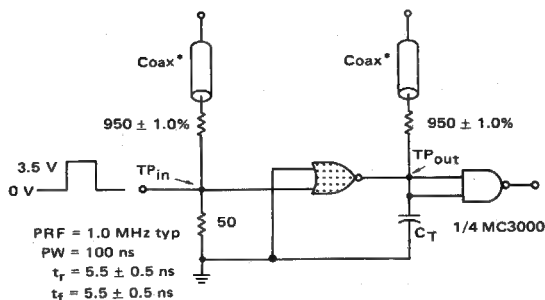
Output Loading Factor = 10

Total Power Dissipation = 122 mW typ/pkg

Propagation Delay Time = 6.0 ns typ

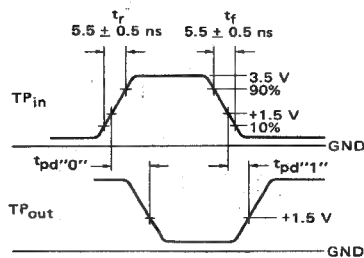
SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



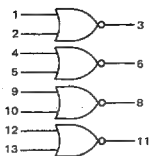
*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@ Test
Temperature

0°C

+25°C

+75°C

Characteristic	Symbol	Pin Under Test	MC3002 Test Limits							TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:															Gnd
			0°C		+25°C		+75°C		Unit																
			Min	Max	Min	Max	Min	Max		I _{OL1}	I _{OL2}	I _{OH}	I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}		
Input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	1	-	2	-	-	14	-	7 *		
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	1	-	2	-	-	-	14	7 *		
Leakage Current	I _R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	1	-	-	-	-	14	2, 7 *		
Breakdown Voltage	BV _{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	14	2, 7 *		
Clamp Voltage	V _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	14	-	7 *		
Output Output Voltage	V _{OL1}	3	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	-	-	1	-	-	-	-	14	-	2, 7 *		
	V _{OL2}	3	-	0.4	-	0.4	-	0.4	Vdc	-	3	-	-	-	-	1	-	-	-	-	-	14	2, 7 *		
	V _{OH}	3	2.5	-	2.5	-	2.5	-	Vdc	-	-	3	-	-	1	-	-	-	-	-	14	-	2, 7 *		
Short-Circuit Current	I _{SC}	3	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	1, 2, 3, 7 *		
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	38	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13		
Power Supply Drain	I _{PDH}	14	-	43	-	43	-	43	mAdc	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	7		
	I _{PDL}	14	-	27	-	27	-	27	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13		
Switching Parameters										Pulse In	Pulse Out														
Turn-On Delay	t _{pd"0"}	1, 3	-	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	-	-	14	-	-	2, 7 *		
Turn-Off Delay	t _{pd"1"}	1, 3	-	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	-	-	14	-	-	2, 7 *		

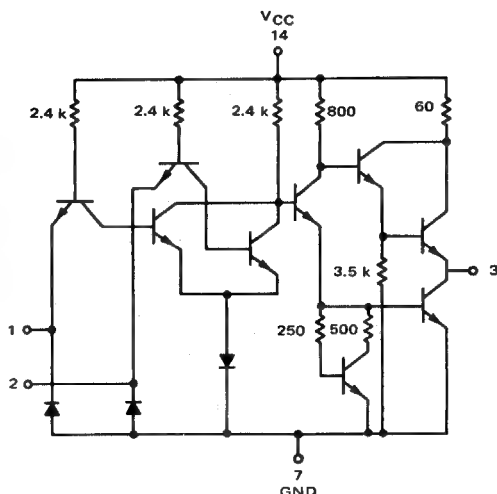
*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

QUAD 2-INPUT "OR" GATE

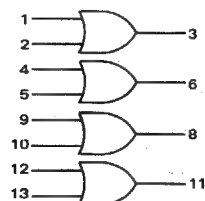
MTTL III MC3000 series

MC3003

1/4 OF CIRCUIT SHOWN



This device consists of four 2-input OR gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.



Positive Logic: $3 = 1 + 2$

Negative Logic: $3 = 1 \cdot 2$

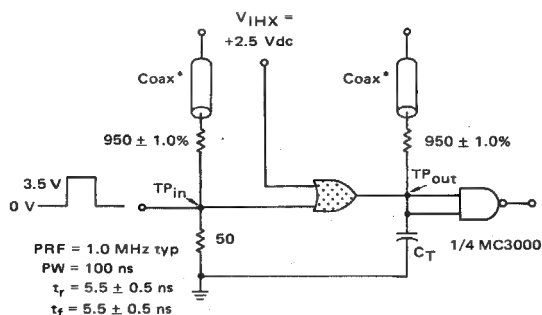
Input Loading Factor = 1

Output Loading Factor = 10

Total Power Dissipation = 150 mW typ/pkg

Propagation Delay Time = 9.0 ns typ

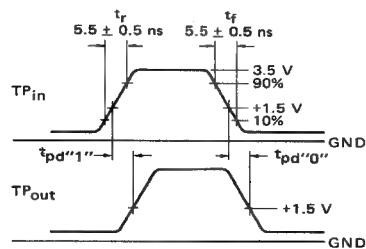
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

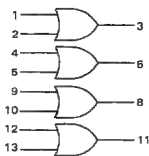
$C_T = 25$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@Test
Temperature
0°C
+25°C
+75°C

TEST CURRENT / VOLTAGE VALUES																	Gnd
mA					Volts												
I _{OL1}	I _{OL2}	I _{OH}	I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	V _{IHX}			
19	23	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5	-			
19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5	2.5			
19	23	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	-			
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																	
I _{OL1}	I _{OL2}	I _{OH}	I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	V _{IHX}			
-	-	-	-	-	-	-	1	-	2 *	-	-	14	-	-	7		
-	-	-	-	-	-	-	1	-	2 *	-	-	-	14	-	7		
-	-	-	-	-	-	-	-	1	*	-	-	-	14	-	2,7		
-	-	-	1	-	-	-	-	-	*	-	-	-	14	-	2,7		
-	-	-	-	1	-	-	-	-	*	-	-	14	-	-	7		
3	-	-	-	-	1	-	-	-	2 *	-	-	14	-	-	7		
-	3	-	-	-	1	-	-	-	2 *	-	-	-	14	-	7		
-	-	3	-	-	-	1	-	-	2 *	-	-	14	-	-	7		
-	-	-	-	-	-	-	-	-	1, 2 *	-	14	-	-	-	3,7		
-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	14	-	-	-	-	7		
-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	-	7		
-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13		
Pulse In	Pulse Out																
1	3	-	-	-	-	-	-	-	*	-	14	-	-	2	7		
1	3	-	-	-	-	-	-	-	*	-	14	-	-	2	7		

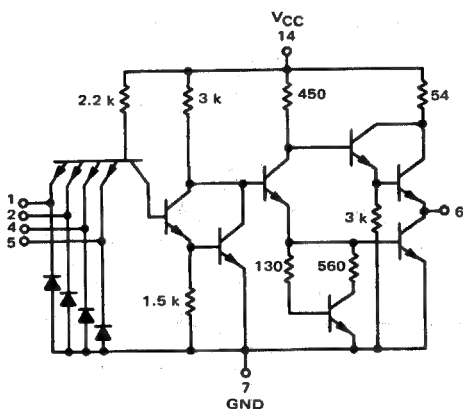
* Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH}

DUAL 4-INPUT "AND" POWER GATE

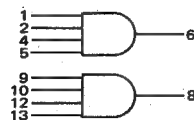
MTTL III MC3000 series

MC3026

1/2 OF CIRCUIT SHOWN



This device consists of two 4-input AND power gates. Each gate is designed for driving high fan-out loads (20).



Positive Logic: $6 = 1 \cdot 2 \cdot 4 \cdot 5$

Negative Logic: $6 = 1 + 2 + 4 + 5$

Input Loading Factor = 1.1

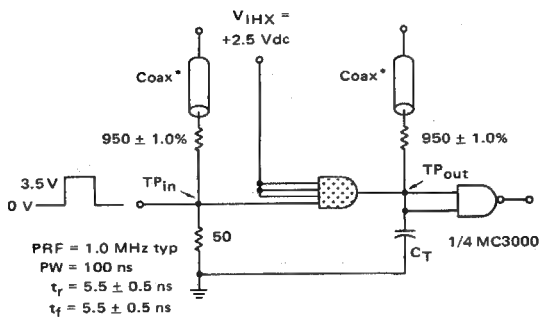
Output Loading Factor = 20

Total Power Dissipation = 90 mW typ/pkg

Propagation Delay Time = 9.0 ns typ

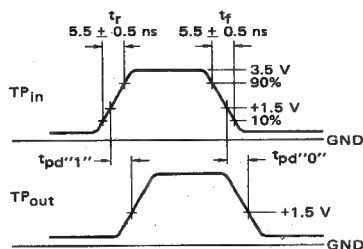
SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



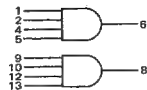
*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@Test
Temperature

0°C

+25°C

+75°C

Characteristic	Symbol	Pin Under Test	MC3026 Test Limits							TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:															Gnd	
			0°C		+25°C		+75°C		Unit																	
			Min	Max	Min	Max	Min	Max		I _{OL1}	I _{OL2}	I _{OH}	I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	V _{IHX}		
Input																										
Forward Current	I _{F1}	1	-	-2.1	-	-2.1	-	-2.1	mAdc	-	-	-	-	-	-	1	-	2, 4, 5 *	-	-	14	-	-	7		
	I _{F2}	1	-	-2.6	-	-2.6	-	-2.6	mAdc	-	-	-	-	-	-	1	-	2, 4, 5 *	-	-	-	14	-	7		
Leakage Current	I _R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	1	*	-	-	-	14	-	2, 4, 5, 7		
Breakdown Voltage	BV _{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	*	-	-	-	14	-	2, 4, 5, 7		
Clamp Voltage	V _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1'	-	-	-	*	-	-	14	-	-	7		
Output	Output Voltage	V _{OL1}	6	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	1	-	-	2, 4, 5 *	-	-	14	-	-	7	
		V _{OL2}	6	-	0.4	-	0.4	-	0.4	Vdc	-	6	-	-	-	1	-	-	2, 4, 5 *	-	-	-	14	-	7	
		V _{OH}	6	2.5	-	2.5	-	2.5	-	Vdc	-	-	6	-	-	-	1	-	-	2, 4, 5 *	-	-	14	-	-	7
Short-Circuit Current	I _{SC}	6	-	-	-50	-125	-	-	mAdc	-	-	-	-	-	-	-	-	1, 2, 4, 5 *	-	14	-	-	-	6, 7		
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	22	-	-	mAdc	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	14	-	-	-	-	7		
	I _{PDH}	14	-	14	-	14	-	14	mAdc	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	-	7		
Power Supply Drain	I _{PDL}	14	-	38	-	38	-	38	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13		
Switching Parameters	Turn-On Delay	t _{pd"0"}	1, 6	-	-	-	15	-	-	ns	Pulse In	Pulse Out	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7		
											1	6														
Turn-Off Delay	t _{pd"1"}	1, 6	-	-	-	15	-	-	ns	1	6	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7		

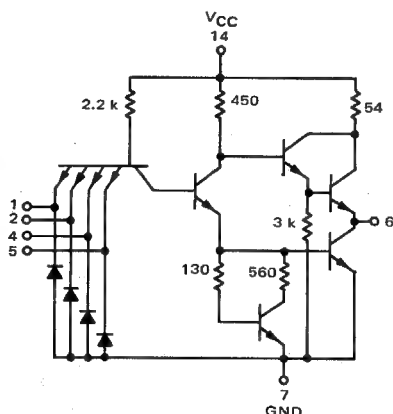
* Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH}.

DUAL 4-INPUT "NAND" POWER GATE

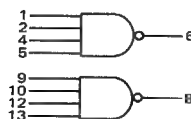
MTTL III MC3000 series

MC3025

1/2 OF CIRCUIT SHOWN



This device consists of two 4-input NAND power gate circuits. Each gate is designed for driving high fan-out loads (20).



$$\text{Positive Logic: } 6 = 1 \cdot 2 \cdot 4 \cdot 5$$

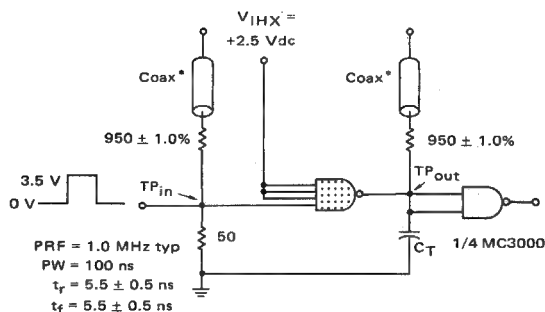
$$\text{Negative Logic: } 6 = 1 + 2 + 4 + 5$$

Input Loading Factor = 1.1
Output Loading Factor = 20

Total Power Dissipation = 70 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

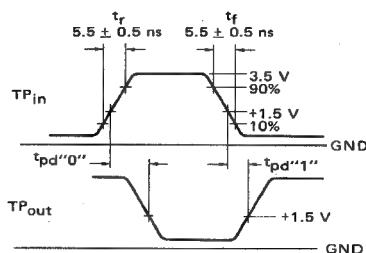
SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



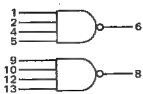
*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@ Test
Temperature
0°C
+25°C
+75°C

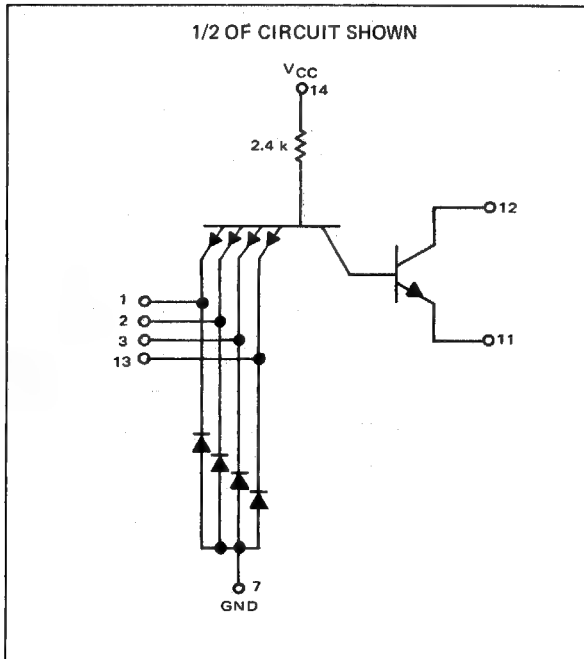
TEST CURRENT / VOLTAGE VALUES																	
mA					Volts												
I _{OL1}	I _{OL2}	I _{OH}	I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	V _{IHX}			
38	46	-4.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5	-			
38	46	-4.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5	2.5			
38	46	-4.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	-			
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																	
I _{OL1}	I _{OL2}	I _{OH}	I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	V _{IHX}	Gnd		
-	-	-	-	-	-	-	1	-	2, 4, 5	-	-	14	-	-	7*		
-	-	-	-	-	-	-	1	-	2, 4, 5	-	-	-	14	-	7*		
-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 4, 5, 7*		
-	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2, 4, 5, 7*		
-	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7*		
6	-	-	-	-	-	1	-	-	2, 4, 5	-	-	14	-	-	7*		
-	6	-	-	-	-	1	-	-	2, 4, 5	-	-	-	14	-	7*		
-	-	6	-	-	1	-	-	-	2, 4, 5	-	-	14	-	-	7		
-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,4,5,6,7*		
-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 4, 5, 7 9,10, 12, 13		
-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	-	7		
-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7 9,10, 12, 13		
Pulse In	Pulse Out																
1	6	-	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*		
1	6	-	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*		

* Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

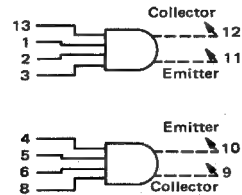
DUAL 4-INPUT EXPANDER FOR "AND-OR-INVERT" GATES

MTTL III MC3000 series

MC3030



This device consists of two independent 4-input AND gates. The outputs of each gate are available as ORing nodes. Using the MC3030 expander, with the MC3020 expandable gate, up to four AND gates can be ORed together.



Input Loading Factor = 1

Full output loading factor of the expandable gate is maintained.

Total Power Dissipation = 15 mW typ/pkg

Propagation Delay Time:

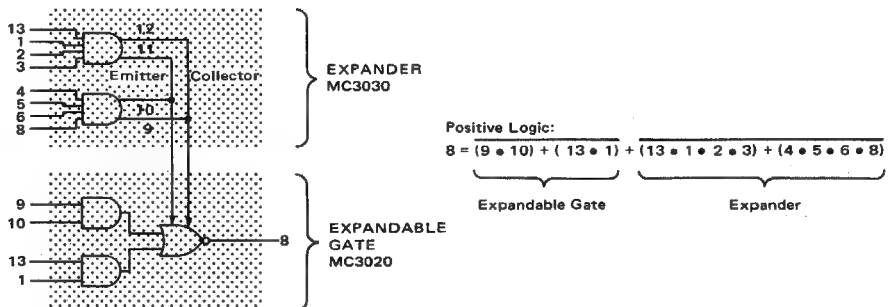
$\Delta t_{pd} = +1.0$ ns typ

When added to the expandable "AND-OR-INVERT" gate.

$\Delta t_{pd}/pF = +1.0$ ns pF typ

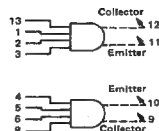
Caused by additional capacitance at expansion points.

APPLICATION: EXPANDABLE 2-WIDE 2-INPUT AND-OR-INVERT GATE WITH A DUAL 4-INPUT EXPANDER CONNECTED



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



@Test
Temperature
0°C
+25°C
+75°C

Characteristic	Symbol	Pin Under Test	MC3030 Test Limits						Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:															Gnd
			0°C		+25°C		+75°C																		
			Min	Max	Min	Max	Min	Max		I _C	I _{In}	I _D	V _R	V _{RH}	V _F	V _{EE1}	V _{EE2}	V _{IH}	V _{IL}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}		
Input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	2, 3, 13	1	-	-	-	-	-	-	14	-	7*	
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	2, 3, 13	1	-	-	-	-	-	-	-	14	7*	
Leakage Current	I _R	1	-	80	-	80	-	80	μAdc	-	-	-	1	-	-	-	-	-	-	-	-	-	14	2, 3, 7, 13*	
Breakdown Voltage	BV _{In}	1	-	-	5.5	-	-	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	-	-	14	2, 3, 7, 13*	
Clamp Voltage	V _D	1	-	-	-	-1.5	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	14	-	7*	
Output Output Voltage	V _{OL}	12	-	1.41	-	1.38	-	1.34	Vdc	12	-	-	-	-	-	11	-	1	-	-	-	14	-	7*	
Emitter Current	I _{EO}	11	-	-300	-	-300	-	-300	μAdc	-	-	-	-	-	-	-	11	-	1	-	-	12, 14	-	7**	
Collector Current	I _{CO}	12	-	300	-	300	-	300	μAdc	-	-	-	-	-	-	-	11	1	-	-	-	12, 14	-	7*	
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	7.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,3,4,5, 6,7,8,13	
Power Supply Drain	I _{PDL}	14	-	5.0	-	5.0	-	5.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	1,2,3,4,5, 6,7,8,13	

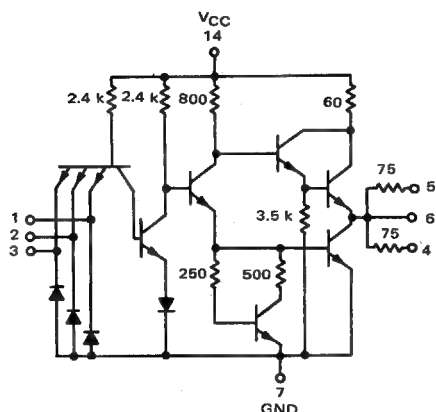
* Ground inputs to gates not under test unless otherwise noted.

** The inputs to both gates are ungrounded.

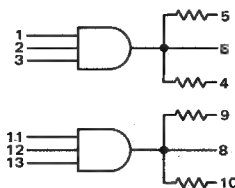
**DUAL 3-INPUT 3-OUTPUT "AND"
SERIES TERMINATED
LINE DRIVER
MC3028**

MTTL III MC3000 series

1/2 OF CIRCUIT SHOWN



This device is a dual 3-input/3-output series-terminated AND line driver that minimizes switching transients on long lines by approximating line impedance. Two outputs are provided through 75-ohm resistors for use when driving 93 to 120-ohm lines. These outputs should be paralleled when driving 50 to 93-ohm lines. In addition, an output is provided directly at the gate output node for driving adjacent gates.



Positive Logic: 4, 5, 6, = $1 \cdot 2 \cdot 3$
Negative Logic: 4, 5, 6, = $1 + 2 + 3$

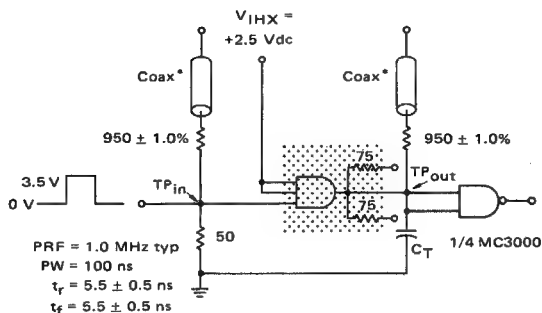
Input Loading Factor = 1

Output Loading Factor, Direct Output (Pins 5 & 8) =
10 minus the number of resistor-terminated outputs
being used.

Output Loading Factor, Resistors (Pins 4, 5, 9, & 10) = 1

Total Power Dissipation = 56 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

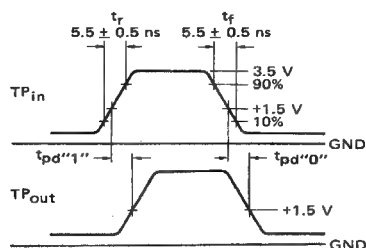
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

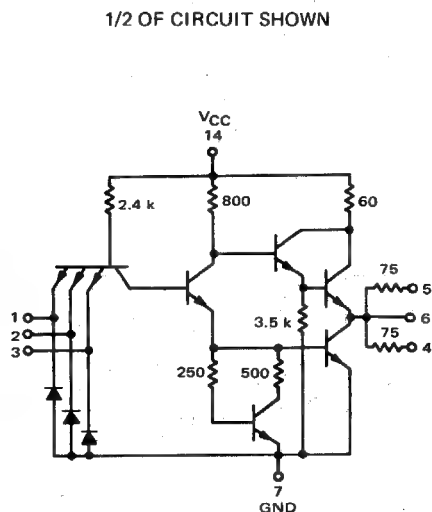
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS

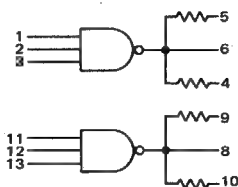


MTTL III MC3000 series

MC3029



This device is a dual 3-input/3-output series-terminated NAND line driver that minimizes switching transients on long lines by approximating line impedance. Two outputs are provided through 75-ohm resistors for use when driving 93 to 120-ohm lines. These outputs should be paralleled when driving 50 to 93-ohm lines. In addition, an output is provided directly at the gate output node for driving adjacent gates.



Positive Logic: $4, 5, 6 = \overline{1 \cdot 2 \cdot 3}$

Negative Logic: $4, 5, 6 = \overline{1 + 2 + 3}$

Input Loading Factor = 1

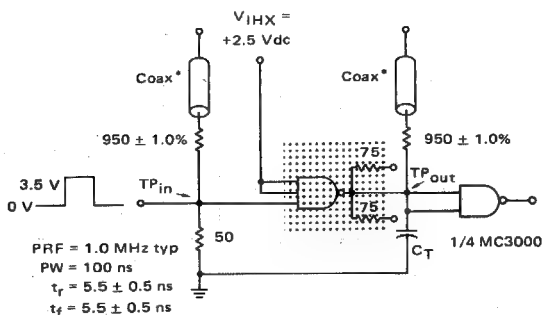
Output Loading Factor, Direct Output (Pins 6 and 8) =
10 Minus The Number of Resistor-Terminated Outputs
Being Used.

Output Loading Factor, Resistors (Pins 4, 5, 9 and 10) = 1

Total Power Dissipation = 44 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

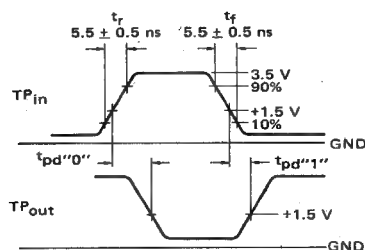
SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



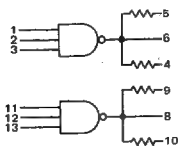
*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one line driver. The other line driver is tested in the same manner. Further, test procedures are shown for only one input of the line driver under test. To complete testing sequence through remaining inputs.



@Test
Temperature
0°C
+25°C
+75°C

				TEST CURRENT/VOLTAGE VALUES																															
				mA								Volts																							
Characteristic	Symbol	Pin Under Test	MC3029 Test Limits								Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:												Gnd											
			0°C		+25°C		+75°C																												
			Min	Max	Min	Max	Min	Max				I _{OL1A}	I _{OL1B}	I _{OL1C}	I _{OL2A}	I _{OL2B}	I _{OL2C}	I _{OH A}	I _{OH B}	I _{OH C}	I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	V _{RHX}			
Input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9			mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	2,3	-	-	14	-	-	7*		
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3			mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	2,3	-	-	-	14	-	7*		
Leakage Current	I _R	1	-	80	-	80	-	80			μAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	-	2,3,7*	
Breakdown Voltage	BV _{in}	1	-	-	5.5	-	-	-			Vdc	-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	-	-	14	-	-	2,3,7*	
Clamp Voltage	V _D	1	-	-	-	-1.5	-	-			Vdc	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	-	14	-	-	7*	
Output Output Voltage	V _{OL1}	6	-	0.4	-	0.4	-	0.4			Vdc	6	5	4	-	-	-	-	-	-	-	-	-	1	-	-	2,3	-	-	14	-	-	7*		
	V _{OL2}	6	-	0.4	-	0.4	-	0.4			Vdc	-	-	-	6	4	5	-	-	-	-	-	-	1	-	-	2,3	-	-	-	14	-	-	7*	
	V _{OL3}	5	-	0.5	-	0.5	-	0.5			Vdc	6	5	4	-	-	-	-	-	-	-	-	1	-	-	2,3	-	-	-	14	-	-	7*		
	V _{OL4}	5	-	0.5	-	0.5	-	0.5			Vdc	-	-	-	6	4	5	-	-	-	-	-	1	-	-	2,3	-	-	-	-	14	-	-	7*	
	V _{OH}	6	2.5	-	2.5	-	2.5	-			Vdc	-	-	-	-	-	-	6	4	5	-	-	1	-	-	-	2,3	-	-	14	-	-	7*		
Short-Circuit Current	I _{SC}	6	-	-	-30	-100	-	-			mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,3,6,7*	
Power Requirements (Total Device)																																			
Maximum Power Supply Current	I _{max}	14	-	-	-	12	-	-			mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	-	1,2,3,7,11,12,13	
Power Supply Drain	I _{PDH}	14	-	18	-	18	-	18			mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1,2,3,11,12,13	-	-	14	-	-	-	7	
	I _{PDL}	14	-	9	-	9	-	9			mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,3,7,11,12,13	
Switching Parameters																																			
	t _{pd"0"}	1,6	-	-	-	10	-	-			ns	Pulse In	Pulse Out																						
Turn-On Delay	t _{pd"0"}	1,6	-	-	-	10	-	-			ns	1	6																					2,3	7*
Turn-Off Delay	t _{pd"1"}	1,6	-	-	-	10	-	-			ns	1	6																					2,3	7*

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

"AND" J-K FLIP-FLOP

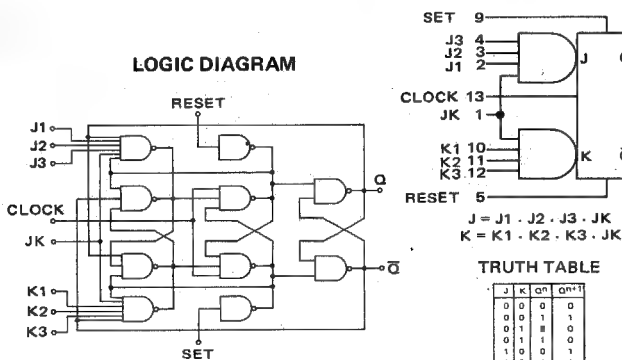
MTTL III MC3000 series

MC3050

This J-K flip-flop triggers on the positive edge of the clock. An AND input gating configuration formed by three J inputs ANDed together and three K inputs ANDed together, minimizes the requirements for external gating. The enable input (JK) consists of a J and a K input internally connected together. This input provides gating for the J and K inputs or an additional logic input for use in counters or other applications. A direct SET and RESET are provided to permit presetting data, such as initial conditions into the flip-flop. The direct SET and RESET fully override the clock; i.e., the direct SET and RESET control the operation of the flip-flop regardless of the state of the clock.

Information may be applied to, or changed at the J and K inputs any time in a clock cycle, except during the interval of time between the Set-up and Hold times. The inputs are inhibited when the clock is high; data is entered into the input steering section of the flip-flop when the clock goes low. The input steering section of the flip-flop continually reflects the input state when the clock is low. Data present during the time interval between the Set-up and Hold times is transferred to the bistable section on the positive edge of the clock and the outputs Q and \bar{Q} respond accordingly. The flip-flop can be set or reset directly by applying the high state to the SET or RESET inputs.

LOGIC DIAGRAM



TRUTH TABLE

J	K	Qn	Qn+1
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Input Loading Factors:

J, K, SET, RESET = 0.6

CLOCK, JK = 1.2

Output Loading Factor = 10

Typical Characteristics ($V_{CC} = 5.0$ V, $T_A = 25^\circ\text{C}$)

Total Power Dissipation = 80 mW/pkg

Toggle Frequency = 40 MHz

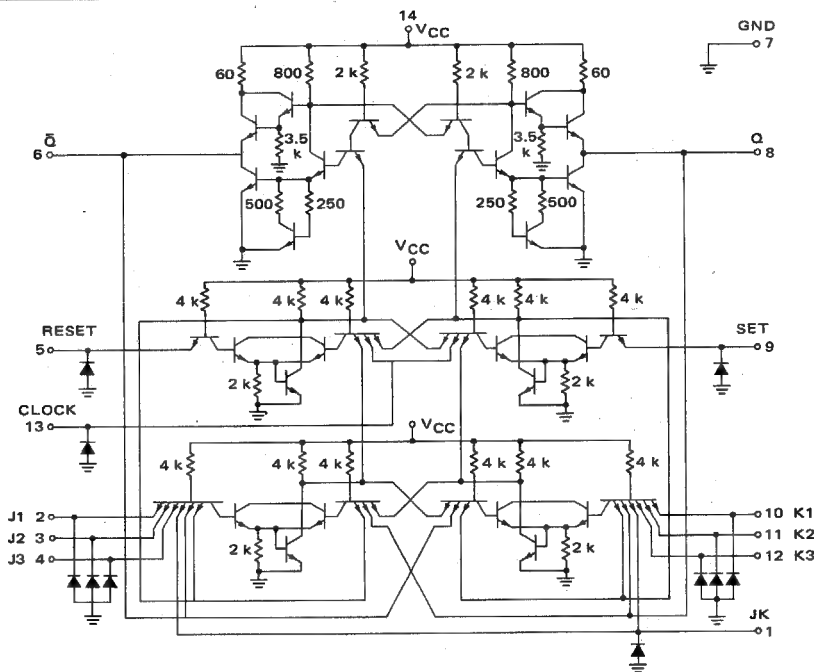
Logical "1" Setup Time = 10 ns

Logical "0" Setup Time = 5.0 ns

Logical "1" and "0" Hold Time = 5.0 ns

t_{pd} "0" = 12 ns

t_{pd} "1" = 14 ns



OPERATING CHARACTERISTICS

High state data must be present 17 ns prior to the rise of the clock and remain 5.0 ns after the clock signal rises.

Positive edge triggering: When the clock goes from the low state to the high state, the information in the input steering section is transferred to the bistable section.

The direct SET and RESET inputs may be used any time, regardless of the state of the clock. If these inputs are not used THEY MUST BE TIED TO GROUND.

Unused Inputs:

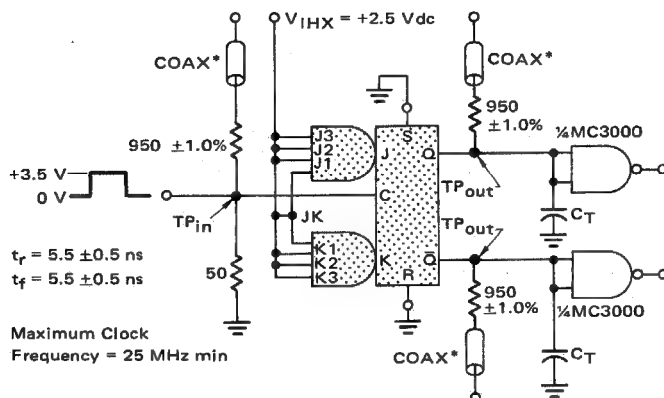
JK input **MUST** be in the high state to enable the clocked inputs. When the JK input is not used, it should be tied to a voltage between 2.0 and 5.5 Vdc.

Unused J inputs should be tied to used J inputs, the used JK input, \bar{Q} , or a voltage between 2.0 and 5.5 Vdc.

Unused K inputs should be tied to used K inputs, the used JK input, Q, or a voltage between 2.0 and 5.5 Vdc.

Unused SET and RESET inputs **MUST** be tied to ground.

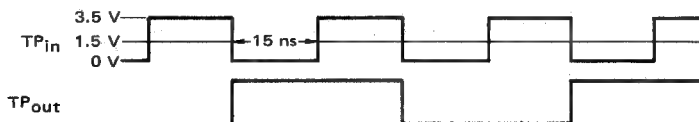
FIGURE 1 – MAXIMUM CLOCK FREQUENCY TEST CIRCUIT

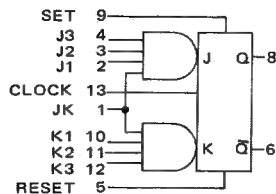


*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

WAVEFORMS AND DEFINITIONS



ELECTRICAL
CHARACTERISTICS

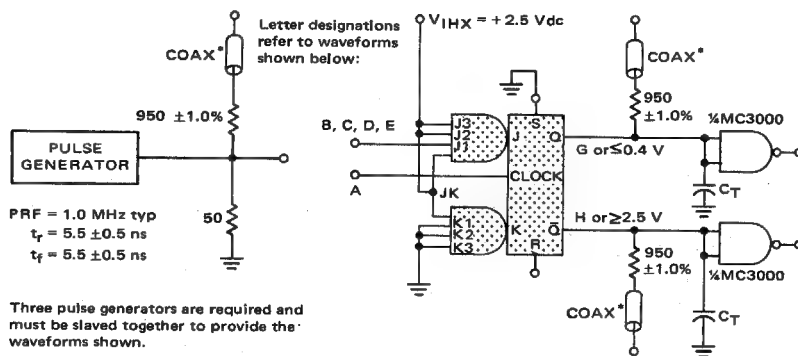
@
Test
Temperature
0°C
+25°C
+75°C

TEST CURRENT/VOLTAGE VALUES													
mA					Volts								
I _{OL}	I _{OH}	I _{in}	2I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}
23	-2.0	-	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5
23	-2.0	1.0	2.0	10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5
23	-2.0	-	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5

Characteristic	Symbol	Pin Under Test	MC3050 Test Limits						Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:													Gnd		
			0°C		+25°C		+75°C			I _{OL}	I _{OH}	I _{In}	2I _{In}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}		V _{CCH}	
			Min	Max	Min	Max	Min	Max																	
Input Forward Current	I _{FJ}	2	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	2	-	1,3,4,5	-	-	-	14	7,9,13	
		3	-	↓	-	↓	-	↓	mAdc	-	-	-	-	-	-	-	3	-	1,2,4,5	-	-	-	↓	↓	
		4	-	↓	-	↓	-	↓	mAdc	-	-	-	-	-	-	-	4	-	1,2,3,5	-	-	-	↓	↓	
	I _{FK}	10	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	10	-	1,9,11,12	-	-	-	14	5,7,13	
		11	-	↓	-	↓	-	↓	mAdc	-	-	-	-	-	-	-	11	-	1,9,10,12	-	-	-	↓	↓	
		12	-	↓	-	↓	-	↓	mAdc	-	-	-	-	-	-	-	12	-	1,9,10,11	-	-	-	↓	↓	
	I _{FC}	13	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	-	13	-	-	-	-	-	14	1,5,7,9	
I _{FJK}	1	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	-	1	-	2,3,4,10,11,12	-	-	-	14	5,7,9,13		
Leakage Current	I _{FS}	9	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	9	-	5	-	-	-	14	7	
		I _{FR}	5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	5	-	9	-	-	-	14	7
			I _{RJ}	2	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	2	-	9	-	-	-	14
	3			-	↓	-	↓	-	↓	μAdc	-	-	-	-	-	-	-	3	-	1,2,4,5,7	-	-	-	↓	↓
	4	-		↓	-	↓	-	↓	μAdc	-	-	-	-	-	-	-	4	-	↓	-	-	-	↓	↓	
	I _{RK}	10	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	10	-	5	-	-	-	14	1,7,9,11,12	
		11	-	↓	-	↓	-	↓	μAdc	-	-	-	-	-	-	-	11	-	↓	-	-	-	↓	↓	
		12	-	↓	-	↓	-	↓	μAdc	-	-	-	-	-	-	-	12	-	↓	-	-	-	↓	↓	
I _{RC}	13	-	110	-	110	-	110	μAdc	-	-	-	-	-	-	-	13	-	1,2,3,4,5,10,11,12	-	-	-	14	7,9		
I _{RJK}	1	-	110	-	110	-	110	μAdc	-	-	-	-	-	-	-	1	-	9	-	-	-	14	2,3,4,5,7,10,11,12		
I _{RS}	9	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	9	-	-	-	-	-	14	7		
I _{RR}	5	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	5	-	-	-	-	-	14	7		

OPERATING CHARACTERISTICS (continued)

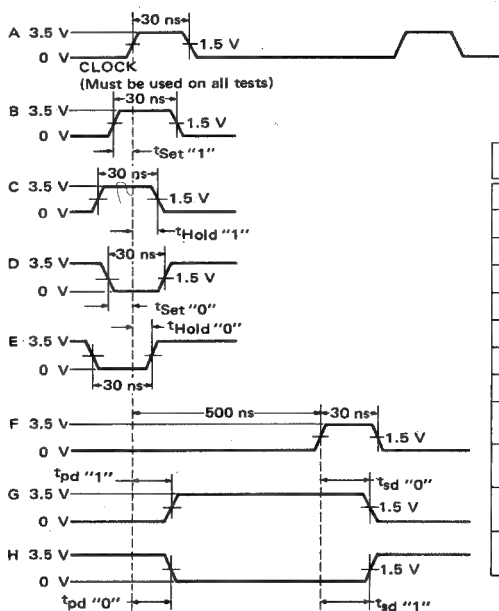
FIGURE 2 – SWITCHING TIME TEST CIRCUIT
(For J inputs and RESET input; to test other inputs, refer to Test Procedures Chart)



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

[illegible]

* Letters shown in these columns refer to waveforms at the left.

τ_{Hold} is typically a negative number.

"AND" INPUT J-K FLIP-FLOP

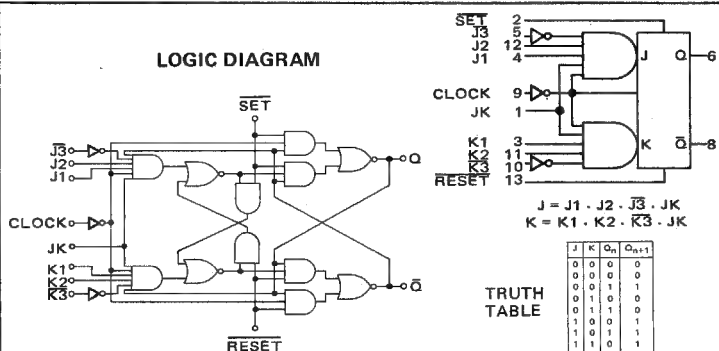
MTTL III MC3000 series

MC3052

The MC3052 is a master-slave J-K flip-flop that triggers on the positive edge of the clock. The flip-flop has an AND input configuration consisting of two J-inputs and a J-input ANDed together and two K-inputs and a K-input ANDed together. An enable input (JK) is also provided consisting of an additional J and K input internally connected together. This input provides gating in addition to the clock for the clocked inputs (J, J, K and K) or an additional logic input (JK) for use in counters or certain other applications. A direct SET and RESET are provided to enable presetting data into the flip-flop such as initial conditions. The direct SET and RESET control the operation of the flip-flop regardless of the state of the clock.

Information is normally applied to, or changed at, the clocked inputs while the clock is in the high state, since the inputs are inhibited under this condition. Information may be stored in the master flip-flop section when the clock goes low. Once input data has been stored in the master flip-flop section it cannot be removed (or changed) by means of the clocked inputs. The direct SET or RESET provide the only means of removing previously stored information. The state of the master flip-flop is transferred to the slave flip-flop section on the positive transition of the clock and the outputs respond accordingly. The flip-flop can be set or reset directly by applying the low state to the direct SET or RESET inputs.

LOGIC DIAGRAM



Input Loading Factors:

$JK = 1.3$
 $J, K, \text{CLOCK} = 0.6$
 $\text{SET}, \text{RESET} = 2.0$

Output Loading Factor = 10

Typical Characteristics:

($V_{CC} = 5.0 \text{ V}$; $T_A = 25^\circ\text{C}$)

Total Power Dissipation = 75 mW/pkg

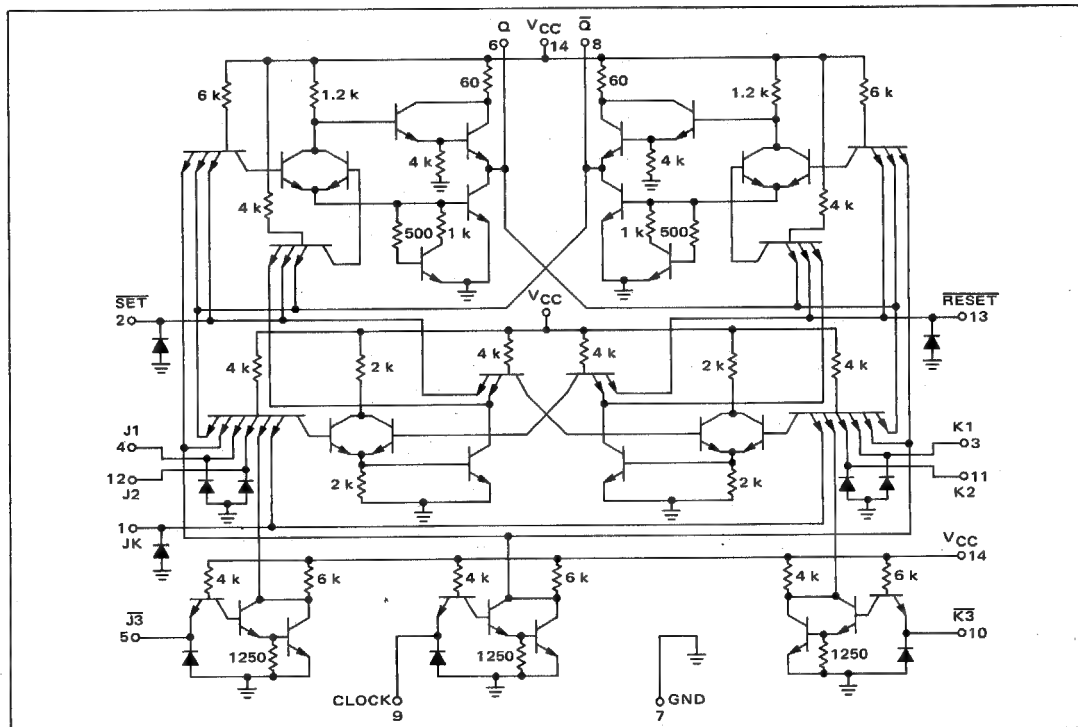
Toggle Frequency = 40 MHz

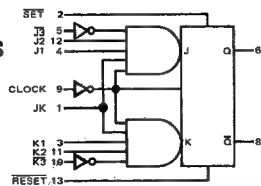
Logical "1" Setup Time = 10 ns

Logical "0" Hold Time = 8.0 ns

$t_{pd} \text{ "0"} = 20 \text{ ns}$

$t_{pd} \text{ "1"} = 12 \text{ ns}$



ELECTRICAL
CHARACTERISTICS

@
Test
Temperature
0°C
+25°C
+75°C

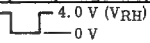
Characteristic	Symbol	Pin Under Test	MC3052 Test Limits						Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:																P ₁ *	Gnd
			0°C		+25°C		+75°C																				
			Min	Max	Min	Max	Min	Max		I _{OL}	I _{OH}	I _{in}	2I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}				
Input Forward Current	I _{FJ}	4 12	- -	-1.5 -1.5	- -	-1.5 -1.5	- -	-1.5 -1.5	mAdc mAdc	- -	- -	- -	- -	- -	- -	- -	4 12	- -	1,12 1,4	- -	- -	- -	14 14	- -	5,7,9,13 5,7,9,13		
	I _{FK}	3 11	- -	-1.5 -1.5	- -	-1.5 -1.5	- -	-1.5 -1.5	mAdc mAdc	- -	- -	- -	- -	- -	- -	- -	3 11	- -	1,11 1,3	- -	- -	- -	14 14	- -	2,7,9,10 2,7,9,10		
	I _{FJ̄}	5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	5	-	-	-	-	-	14	-	7		
	I _{FK̄}	10	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	10	-	-	-	-	-	14	-	7		
	I _{FC}	9	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	9	-	-	-	-	-	14	-	7		
	I _{FJK}	1	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	-	1	-	3,4,11,12	-	-	-	14	-	2,5,7,9,10,13		
	I _{F̄S}	2	-	-4.5	-	-4.5	-	-4.5	mAdc	-	-	-	-	-	-	-	2	-	-	-	-	-	14	-	7,9,13		
	I _{F̄R}	13	-	-4.5	-	-4.5	-	-4.5	mAdc	-	-	-	-	-	-	-	13	-	-	-	-	-	14	-	2,7,9		
Leakage Current	I _{RJ}	4 12	- -	80 80	- -	80 80	- -	80 80	μAdc μAdc	- -	- -	- -	- -	- -	- -	- -	4 12	- -	5,9 5,9	- -	- -	- -	14 14	- -	1,2,7,12 1,2,4,7		
	I _{RK}	3 11	- -	80 80	- -	80 80	- -	80 80	μAdc μAdc	- -	- -	- -	- -	- -	- -	- -	3 11	- -	9,10 9,10	- -	- -	- -	14 14	- -	1,7,11,13 1,3,7,13		
	I _{RJ̄}	5	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	5	-	-	-	-	-	14	-	7		
	I _{RK̄}	10	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	10	-	-	-	-	-	14	-	7		
	I _{RC}	9	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	9	-	-	-	-	-	14	-	7		
	I _{RJK}	1	-	110	-	110	-	110	μAdc	-	-	-	-	-	-	-	1	-	5,9,10	-	-	-	14	-	3,4,6,7,8,11,12		
	I _{R̄S}	2	-	140	-	140	-	140	μAdc	-	-	-	-	-	-	-	2	-	1,4,10,12,13	-	-	-	14	9	3,5,7,11		
	I _{R̄R}	13	-	140	-	140	-	140	μAdc	-	-	-	-	-	-	-	13	-	1,2,3,5,11	-	-	-	14	9	4,7,10,12		

*Pulse is used to set flip-flop in desired state. P₁ = 4.0 V (V_{RH})
0 V

**ELECTRICAL
CHARACTERISTICS (continued)**

@
Test
Temperature

TEST CURRENT/VOLTAGE VALUES															
mA					Volts										
I _{OL}	I _{OH}	I _{in}	2I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}		
23	-2.0	-	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5		
23	-2.0	1.0	2.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5		
23	-2.0	-	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5		
TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:															
I _{OL}	I _{OH}	I _{in}	2I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	P ₁ *	Gnd
-	-	4	-	-	-	-	-	-	5,9	-	-	-	14	-	1,2,7,12
-	-	12	-	-	-	-	-	-	5,9	-	-	-	↓	-	1,2,4,7
-	-	3	-	-	-	-	-	-	9,10	-	-	-	-	-	1,7,11,13
-	-	11	-	-	-	-	-	-	9,10	-	-	-	-	-	1,3,7,13
-	-	1	-	-	-	-	-	-	2,5,9,10,13	-	-	-	-	-	3,4,6,7,8,11,12
-	-	2	-	-	-	-	-	-	1,4,10,12,13	-	-	-	-	9	3,5,7,11
-	-	13	-	-	-	-	-	-	1,2,3,5,11	-	-	-	-	9	4,7,10,12
-	-	5	-	-	-	-	-	-	-	-	-	-	-	-	7
-	-	9	-	-	-	-	-	-	-	-	-	-	-	-	7
-	-	10	-	-	-	-	-	-	-	-	-	-	↓	-	7
-	-	-	-	4	-	-	-	-	-	-	-	14	-	-	7
-	-	-	-	12	-	-	-	-	-	-	-	↓	-	-	↓
-	-	-	-	3	-	-	-	-	-	-	-	-	-	-	↓
-	-	-	-	11	-	-	-	-	-	-	-	-	-	-	↓
-	-	-	-	5	-	-	-	-	-	-	-	-	-	-	↓
-	-	-	-	10	-	-	-	-	-	-	-	-	-	-	↓
-	-	-	-	9	-	-	-	-	-	-	-	-	-	-	↓
-	-	-	-	1	-	-	-	-	-	-	-	-	-	-	↓
-	-	-	-	2	-	-	-	-	-	-	-	↓	-	-	↓
-	-	-	-	13	-	-	-	-	-	-	-	-	-	-	↓
6	-	-	-	-	13	2	-	-	-	-	-	-	14	-	7,9
8	-	-	-	-	2	13	-	-	-	-	-	-	14	-	7,9
-	6	-	-	-	2	13	-	-	-	-	-	14	-	-	7,9
-	8	-	-	-	13	2	-	-	-	-	-	14	-	-	7,9
-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	2,6,7
-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	7,8,13
-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1,2,3,4,5,7,9,10,11,12,13
-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,5,7,9,10

*Pulse is used to set flip-flop in desired state. P₁ =  4.0 V (VRH)
0 V

OPERATING CHARACTERISTICS

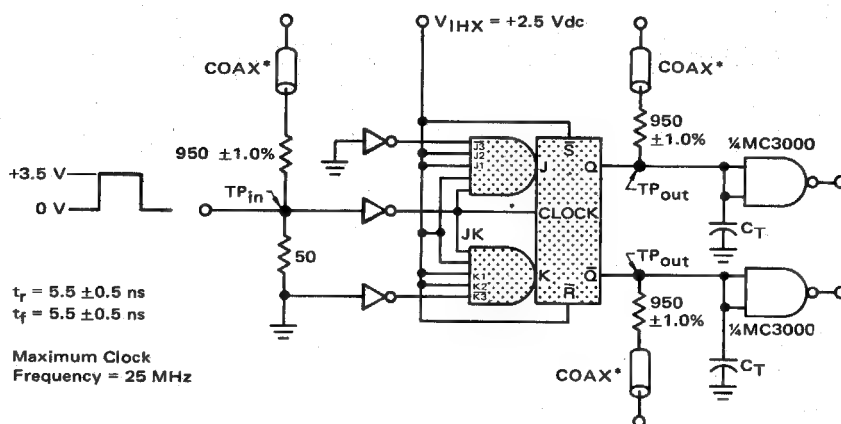
Data should be present prior to the negative clock transition. If data is changed from a "1" to a "0" while the clock is in the low state, the flip-flop will not recognize this new data state.

The application of a low level to the $\overline{\text{SET}}$ input sets Q high and low level on the $\overline{\text{RESET}}$ input resets Q low. These functions may be performed at any time without regard to the clock area.

Positive edge triggering — When the clock goes from the low to the high state, the information stored in the master flip-flop section is transferred to the slave flip-flop section thus appearing at the outputs. When the clock is in the high state, the inputs are inhibited.

Unused J, K, and JK inputs should be tied together with used inputs, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc. The unused $\overline{\text{J}}$ and $\overline{\text{K}}$ inputs must be tied to ground. The unused $\overline{\text{SET}}$ and $\overline{\text{RESET}}$ inputs should be tied to a voltage between 2.0 and 5.5 Vdc.

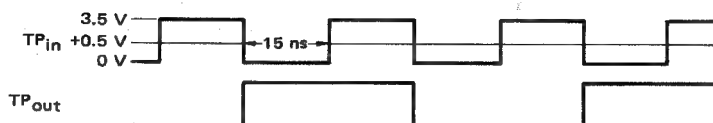
FIGURE 1 — MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

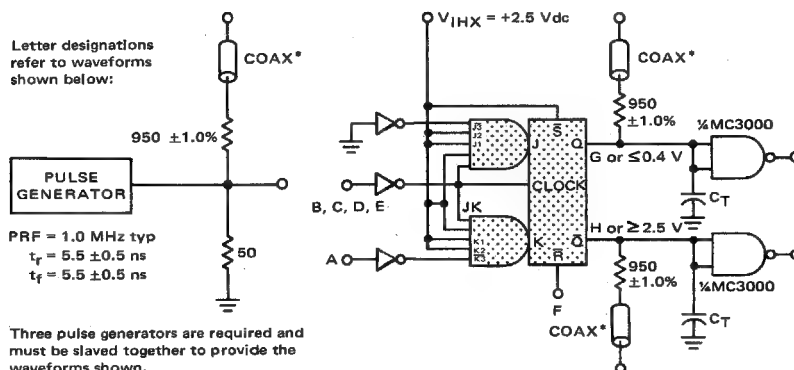
WAVEFORMS AND DEFINITIONS



OPERATING CHARACTERISTICS (continued)

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

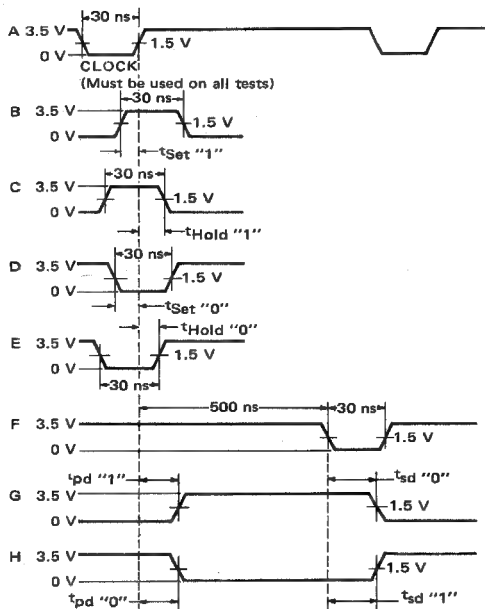
(For J inputs and RESET input: to test other inputs, refer to Test Procedures Chart)



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

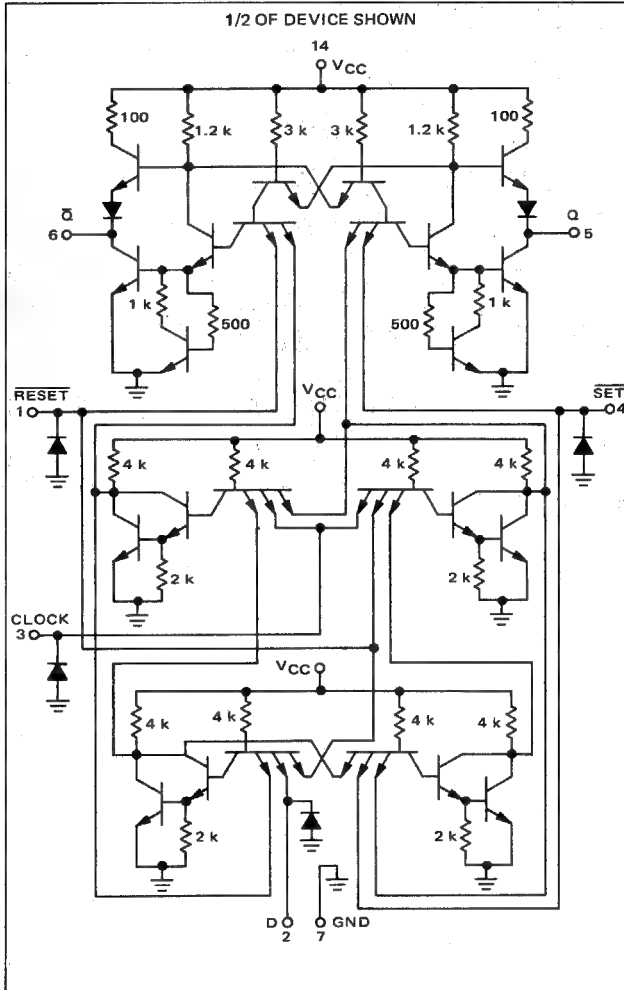
TEST	INPUT						Q*	Q̄*	LIMITS (ns)	
	J*	J*	SET*	RESET*	K*	R*			Min	Max
†Set "1"	J	C	Gnd	2.5 V	F	Gnd	G	H	—	15
†Hold "0"	J	B	Gnd	2.5 V	F	Gnd	≤0.4 V	≥2.5 V	—	—3.0
†Set "1"	K	Gnd	Gnd	F	2.5 V	C	Gnd	H	Q	—15
†Hold "0"	K	Gnd	Gnd	F	2.5 V	B	Gnd	≥2.5 V	≤0.4 V	— —3.0
†Set "1"	J	2.5 V	E	2.5 V	†F	2.5 V	Gnd	Q	H	—15
†Hold "0"	J	2.5 V	D	2.5 V	F	2.5 V	Gnd	≤0.4 V	≥2.5 V	— —3.0
†Set "1"	R	2.5 V	Gnd	F	2.5 V	2.5 V	E	H	Q	—15
†Hold "0"	R	2.5 V	Gnd	F	2.5 V	2.5 V	D	≥2.5 V	≤0.4 V	— —3.0
†pd "1"			Delay from clock to Q during †Set "1" J test. Delay from clock to Q during †Set "1" K test.						8	20
†pd "0"			Delay from clock to Q̄ during †Set "1" J test. Delay from clock to Q during †Set "1" K test.						14	28
†pd "1"			Delay from SET to Q during †Set "1" K test. Delay from RESET to Q during †Set "1" J test.						—	18
†pd "0"			Delay from SET to Q̄ during †Set "1" K test. Delay from RESET to Q during †Set "1" J test.						—	25

*Letters shown in these columns refer to waveforms.

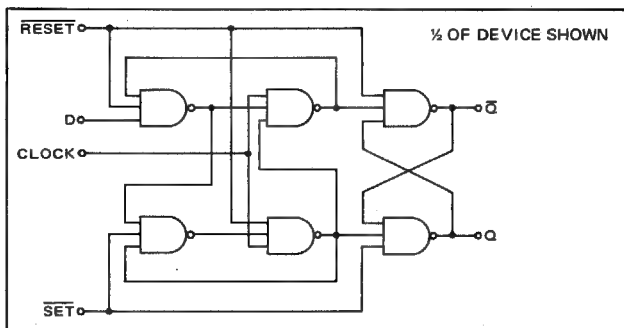
DUAL TYPE D FLIP-FLOP

MTTL III MC3000 series

MC3060



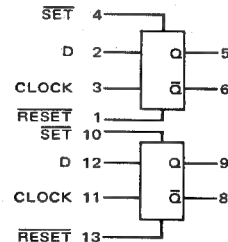
LOGIC DIAGRAM



The MC3060 dual flip-flop triggers on the positive edge of the clock and performs the Type D flip-flop logic function. This device consists of two completely independent Type D flip-flops, both having direct SET and RESET inputs for asynchronous operations such as parallel data entry in shift register applications.

Information may be applied to, or changed at, the D inputs any time during the clock cycle except during the time interval between the Set-up and Hold times. The clocked inputs are inhibited when the clock is high and data may be applied to the input steering section of the flip-flop when the clock goes low. The input steering section continually reflects the input state being applied when the clock is low. The information present at the inputs during the time interval between the Set-up and Hold times is transferred to the bistable section on the positive edge of the clock, and the outputs Q and \bar{Q} respond accordingly.

The flip-flop can also be set or reset directly at any time, regardless of the state of the clock, by applying a low state to the direct SET or RESET inputs.



TRUTH TABLE

D	Q^n	Q^{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$$Q^{n+1} = D^n$$

Input Loading Factors:

SET = 1.0
RESET = 1.5
CLOCK = 1.4
D = 0.6

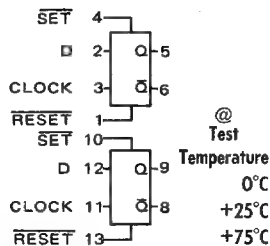
Output Loading Factor = 10

Typical Characteristics: ($V_{CC} = 5.0$ V, $T_A = 25^\circ\text{C}$)

Total Power Dissipation = 120 mW/pkg
Toggle Frequency = 30 MHz
Logical "1" Setup Time = 10 ns
Logical "0" Setup Time = 5.0 ns
Logical "1" and "0" Hold Times = 5.0 ns
 t_{pd} "0" = 17 ns
 t_{pd} "1" = 15 ns

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



TEST CURRENT/VOLTAGE VALUES															P ₁ [*]	Gnd	
mA					Volts												
I _{OL}	I _{OH}	I _{in}	2I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}				
23	-2.0	-	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5				
23	-2.0	1.0	2.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5				
23	-2.0	-	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5				
TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:																	
I _{OL}	I _{OH}	I _{in}	2I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}				
-	-	-	-	-	-	-	3	-	1	-	-	-	14	-			2,4,7,11
-	-	-	-	-	-	-	2	-	1,4	-	-	-	14	-			3,7,11
-	-	-	-	-	-	-	4	-	1	-	-	-	14	-	2,3,7,11		
-	-	-	-	-	-	-	1	-	2,4	-	-	-	14	-	3,7,11		
-	-	-	-	-	-	-	-	3	4	-	-	-	14	-	1,2,7,11		
-	-	-	-	-	-	-	-	2	3,4	-	-	-	14	-	1,7,11		
-	-	-	-	-	-	-	-	4	1,2	-	-	-	14	3	7,11		
-	-	-	-	-	-	-	-	1	4	-	-	-	14	3	2,7,11		
-	-	-	3	-	-	-	-	-	4	-	-	-	14	-	1,2,7,11		
-	-	2	-	-	-	-	-	-	3,4	-	-	-	↓	-	1,7,11		
-	-	-	4	-	-	-	-	-	1,2	-	-	-	-	3	7,11		
-	-	-	1	-	-	-	-	-	4	-	-	-	↓	3	2,7,11		
-	-	-	-	3	-	-	-	-	-	-	-	14	-	-	7,11		
-	-	-	-	2	-	-	-	-	-	-	-	↓	-	-	↓		
-	-	-	-	4	-	-	-	-	-	-	-	-	-	-	-		
-	-	-	-	1	-	-	-	-	-	-	-	↓	-	-	↓		
6	-	-	-	-	4	1	-	-	-	-	-	-	14	-	2,3,7,11		
5	-	-	-	-	1	4	-	-	-	-	-	-	14	-	2,3,7,11		
-	6	-	-	-	1	4	-	-	-	-	-	14	-	-	2,3,7,11		
-	5	-	-	-	4	1	-	-	-	-	-	14	-	-	2,3,7,11		
-	-	-	-	-	-	4	1	-	-	-	14	-	-	-	6,7,11		
-	-	-	-	-	-	1	4	-	-	-	14	-	-	-	5,7,11		
-	-	-	-	-	-	-	-	-	1,13	14	-	-	-	-	3,4,7,10,11		
-	-	-	-	-	-	-	-	-	4,10	-	14	-	-	-	1,3,7,11,13		

* Pulse is used to set flip-flop in desired state. P₁ = 4.0 V (V_{RH}). If pin is also in another column, the pin must be returned to that voltage or current for measurement.

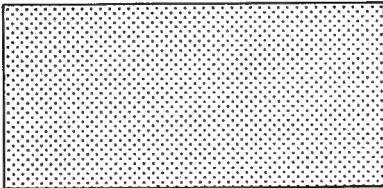
OPERATING CHARACTERISTICS

Data must be present 15 ns prior to the rise of the clock and remain 5.0 ns after the clock signal rises.

The direct $\overline{\text{SET}}$ and $\overline{\text{RESET}}$ inputs may be used at any time as they completely override the clock.

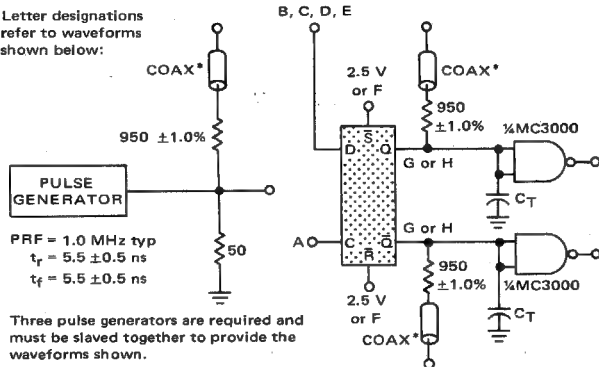
Positive edge triggering: When the clock goes from the low to the high state, the information in the input steering section is transferred to the bistable section.

Unused inputs should be tied to a voltage between 2.0 and 5.5 Vdc.



SWITCHING TIME TEST CIRCUIT

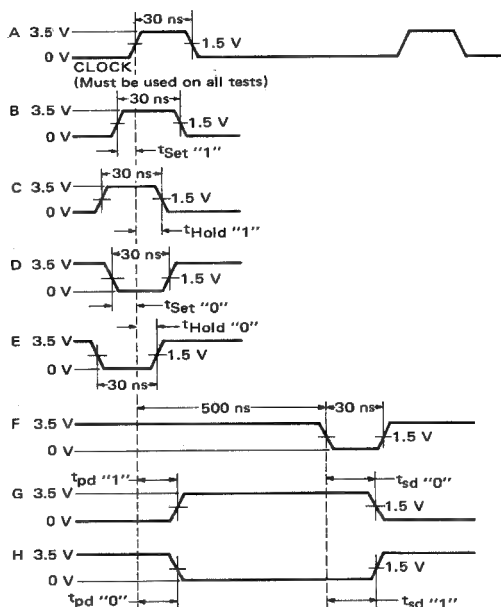
Letter designations refer to waveforms shown below:



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST	INPUT				Q*	\overline{Q} *	LIMITS (ns)	
	D*	SET*	RESET*				Min	Max
$t_{\text{Set}} "1"$	D	B	2.5 V	F	G	H	—	15
$t_{\text{Hold}} "1"$	D	C	2.5 V	F	G	H	—	5.0
$t_{\text{Set}} "0"$	D	D	F	2.5 V	H	G	—	15
$t_{\text{Hold}} "0"$	D	E	F	2.5 V	H	G	—	5.0
$t_{\text{pd}} "1"$	Delay from clock to Q during $t_{\text{Set}} "1"$ D test. Delay from clock to \overline{Q} during $t_{\text{Set}} "0"$ D test.						10	25
$t_{\text{pd}} "0"$	Delay from clock to Q during $t_{\text{Set}} "0"$ D test. Delay from clock to \overline{Q} during $t_{\text{Set}} "1"$ D test.						10	25
$t_{\text{sd}} "1"$	Delay from SET to Q during $t_{\text{Set}} "0"$ D test. Delay from RESET to \overline{Q} during $t_{\text{Set}} "1"$ D test.						5.0	20
$t_{\text{sd}} "0"$	Delay from SET to \overline{Q} during $t_{\text{Set}} "0"$ D test. Delay from RESET to Q during $t_{\text{Set}} "1"$ D test.						5.0	20

*Letters shown in these columns refer to waveforms at left.

DUAL J-K FLIP-FLOP

MTTL III MC3000 series

MC3061

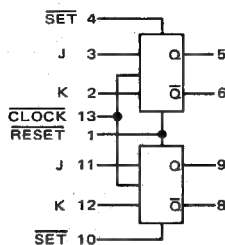
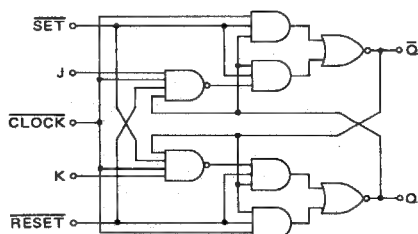
The MC3061 dual JK flip-flop triggers on the negative edge of the clock. Each flip-flop is provided with a separate direct SET input in addition to the common direct RESET input. These direct inputs provide a means of resetting a group of flip-flops such as a register which may be followed by the presetting of a data pattern. The clock input for this device is common for both flip-flops, making it particularly useful in registers or other common clock applications.

Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between

the Setup and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between the Setup and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at any time without regard to the clock state by applying a low level to the SET input. In addition, both flip-flops may be reset simultaneously by using the common RESET in a similar manner.

LOGIC DIAGRAM

1/2 OF DEVICE SHOWN,
RESET AND CLOCK COMMON TO BOTH



Input Loading Factors:

SET = 1.6

RESET, CLOCK = 3.2

J, K = 0.6

Output Loading Factor = 10

J-K TRUTH TABLE

J	K	Q ⁿ	Q ⁿ⁺¹
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Typical Characteristics

(V_{CC} = 5.0 V; T_A = 25°C)

Total Power Dissipation = 100 mW/pkg

Toggle Frequency = 50 MHz

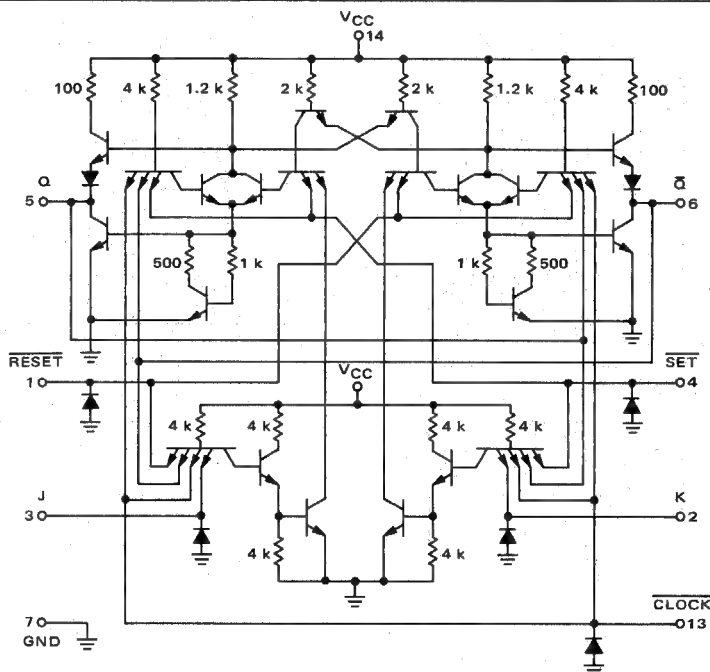
Logical "1" Setup Time = 8.0 ns

Logical "0" Setup Time = 8.0 ns

Logical "1" and "0" Hold Times = 0 ns

t_{pd} "0" = 12 ns

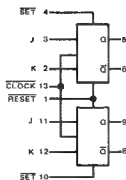
t_{pd} "1" = 12 ns



1/2 OF CIRCUIT
SHOWN (RESET AND CLOCK
COMMON TO BOTH)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop plus the inputs common to both flip-flops. To complete testing, sequence through the remaining inputs in the same manner.



@
Test
Temperature
0°C
+25°C
+75°C

TEST CURRENT/VOLTAGE VALUES													
mA					Volts								
I _{OL}	I _{OH}	I _{in}	2I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}
23	-2.0	-	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5
23	-2.0	1.0	2.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5
23	-2.0	-	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5

Characteristic	Symbol	Pin Under Test	MC3061 Test Limits						Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:														P ₁ *	Gnd
			0°C		+25°C		+75°C			I _{OL}	I _{OH}	I _{in}	2I _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}		
			Min	Max	Min	Max	Min	Max																	
Input Forward Current	I _{FJ}	3	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	3	-	1,4,13	-	-	-	14	1	2,7,10	
	I _{FK}	2	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	2	-	1,4,13	-	-	-	14	4	3,7,10	
	I _{FR}	1	-	-3.5	-	-3.5	-	-3.5	mAdc	-	-	-	-	-	-	1	-	3,4,13	-	-	-	14	-	2,7,10	
	I _{FS}	4	-	-1.8	-	-1.8	-	-1.8	mAdc	-	-	-	-	-	-	4	-	1,2,13	-	-	-	14	-	3,7,10	
	I _{FC}	13	-	-5.7	-	-5.7	-	-5.7	mAdc	-	-	-	-	-	-	13	-	1,2,3,11,12	-	-	-	14	4,10	7	
Leakage Current	I _{RJ}	3	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	3	2,4	-	-	-	14	-	1,7,10,13		
	I _{RK}	2	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	2	1,3	-	-	-	14	-	4,7,10,13		
	I _{RR}	1	-	230	-	230	-	230	μAdc	-	-	-	-	-	-	1	2	-	-	-	14	1	3,4,7,11,13		
	I _{RS}	4	-	140	-	140	-	140	μAdc	-	-	-	-	-	-	4	3	-	-	-	14	4	1,2,7,10,13		
	I _{RC}	13	-	290	-	290	-	290	μAdc	-	-	-	-	-	-	13	-	-	-	-	14	-	1,2,3,4,7,10,11,12		
Breakdown Voltage	BV _{in}	3	-	-	5.5	-	-	-	Vdc	-	-	3	-	-	-	-	-	2,4	-	-	-	14	-	1,7,10,13	
		2	-	-	-	-	-	-	Vdc	-	-	2	-	-	-	-	-	1,3	-	-	-	-	-	4,7,10,13	
		1	-	-	-	-	-	-	Vdc	-	-	-	1	-	-	-	-	2	-	-	-	-	1	3,4,7,11,13	
		4	-	-	-	-	-	-	Vdc	-	-	-	4	-	-	-	-	3	-	-	-	-	4	1,2,7,10,13	
		13	-	-	↓	-	-	-	Vdc	-	-	-	13	-	-	-	-	-	-	-	-	↓	-	1,2,3,4,7,10,11,12	
Clamp Voltage	V _D	3	-	-	-	-1.5	-	-	Vdc	-	-	-	-	3	-	-	-	-	-	-	-	14	-	7,10	
		2	-	-	-	-	-	-	Vdc	-	-	-	-	2	-	-	-	-	-	-	-	-	-	-	
		1	-	-	-	-	-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	-	-	-	-	
		4	-	-	-	-	-	-	Vdc	-	-	-	-	4	-	-	-	-	-	-	-	-	-	-	
		13	-	-	-	↓	-	-	Vdc	-	-	-	-	13	-	-	-	-	-	-	-	↓	-	-	
Output Output Voltage	V _{OL}	5	-	0.4	-	0.4	-	0.4	Vdc	5	-	-	-	-	1	4	-	-	-	-	-	14	1	7,10	
		6	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	4	1	-	-	-	-	-	14	4	7,10	
	V _{OH}	5	2.5	-	2.5	-	2.5	-	Vdc	-	5	-	-	-	4	1	-	-	-	-	-	14	-	4	7,10
		6	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	-	4	1	-	-	-	-	-	14	1	7,10	
Short-Circuit Current	I _{SC}	5	-	-	-20	-60	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	4,5,7,10
		6	-	-	-20	-60	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1,6,7,10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	42	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	-	-	4,7,10
Power Supply Drain	I _{PD}	14	-	30	-	30	-	30	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1,7

*Momentarily ground pin prior to taking measurement. (If pin is also in another column, the pin must be returned to that voltage or current for measurement.)

MC3061 (continued)

OPERATING CHARACTERISTICS

High state data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

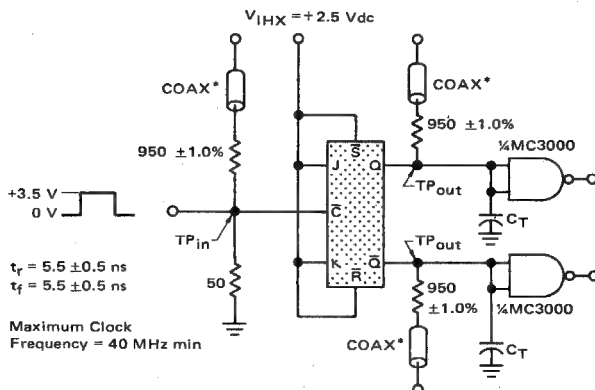
The direct SET (individual) inputs and RESET (common) inputs may be used at any time without regard to the clock state. The flip-flop is set to the $Q = 1$ state by applying a low level to the SET input or reset to the $Q = 0$ state by applying a low level to the RESET input. If these inputs are not used they should be returned to a voltage level that is not specified.

age between 2.0 and 5.5 Vdc.

Negative edge triggering — The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low.

Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.

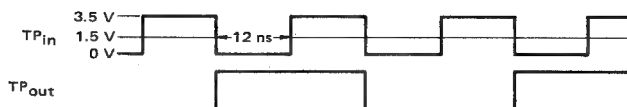
MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

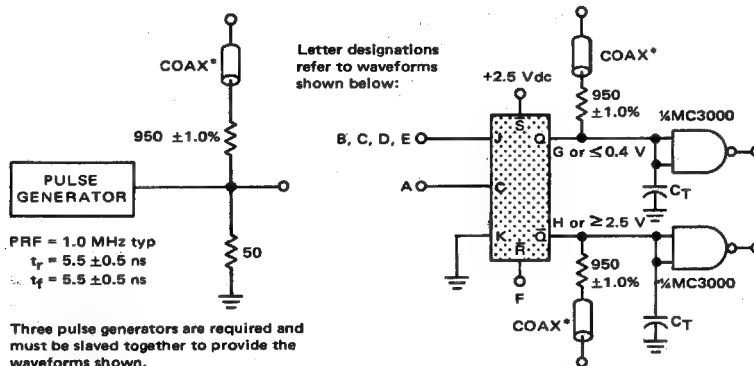
VOLTAGE WAVEFORMS AND DEFINITIONS



OPERATING CHARACTERISTICS (continued)

SWITCHING TIME TEST CIRCUIT

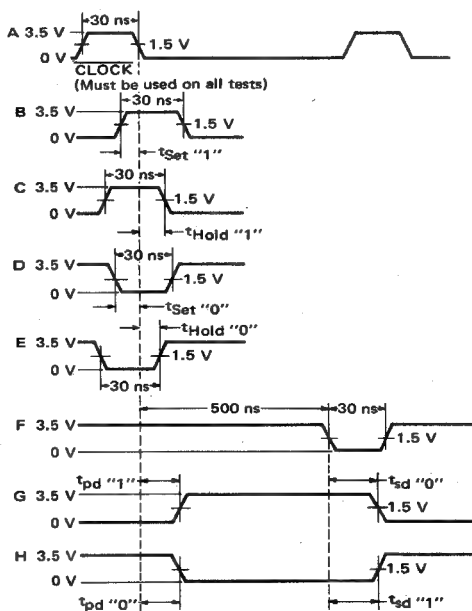
(For J Inputs and RESET Input; to test other inputs, refer to Test Procedures Chart)



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST	INPUT				Q*	Q*	LIMITS (ns)
	J*	SET*	RESET*	K*			
*Set "1"	J	B	2.5 V	F	Gnd	G	H 15
*Hold "1"	J	C	2.5 V	F	Gnd	G	H 0**
*Set "0"	J	D	2.5 V	F	Gnd	≤0.4 V	22.5 V 15
*Hold "0"	J	E	2.5 V	F	Gnd	≤0.4 V	22.5 V 0**
*Set "1"	K	Gnd	F	2.5 V	B	H	G 15
*Hold "1"	K	Gnd	F	2.5 V	C	H	G 0**
*Set "0"	K	Gnd	F	2.5 V	D	22.5 V	≤0.4 V 15
*Hold "0"	K	Gnd	F	2.5 V	E	22.5 V	≤0.4 V 0**
*t _{pd} "1"	Delay from clock to Q during "Set "1" J test.				Delay from clock to Q during "Set "1" K test.		15
*t _{pd} "0"	Delay from clock to Q during "Set "1" J test.				Delay from clock to Q during "Set "1" K test.		15
*t _{pd} "1"	Delay from SET to Q during "Set "1" K test.				Delay from RESET to Q during "Set "1" J test.		15
*t _{pd} "0"	Delay from SET to Q during "Set "1" K test.				Delay from RESET to Q during "Set "1" J test.		15

*Letters shown in these columns refer to waveforms shown at the left.

**t_{hold} is typically a negative number.

DUAL J-K FLIP-FLOP

MTTL III MC3000 series

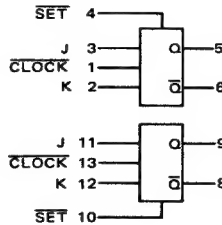
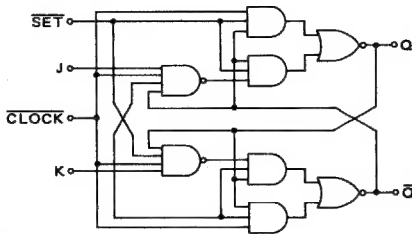
MC3062

The MC3062 dual JK flip-flop triggers on the negative edge of the clock. Each flip-flop is provided with a separate direct SET input. These direct inputs provide a means of presetting the flip-flop to initial conditions or other asynchronous operations.

Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between

the Set-up and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between Set-up and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at anytime without regard to the clock state by applying a low level to the SET input.

LOGIC DIAGRAM
1/2 OF DEVICE SHOWN



Input Loading Factors:
CLOCK, SET = 1.6
J, K, = 0.6

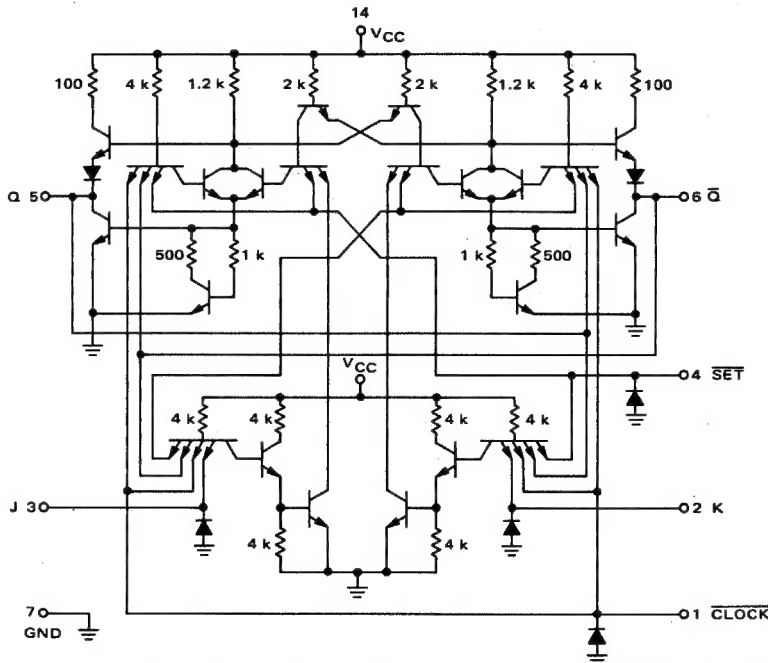
Output Loading Factor = 10

J-K TRUTH TABLE

J	K	Qn	Qn+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Typical Characteristics:
($V_{CC} = 5.0 \text{ V}$; $T_A = 25^\circ\text{C}$)

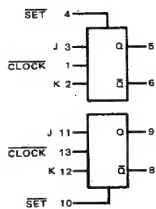
Total Power Dissipation = 100 mW/pkg
Toggle Frequency = 50 MHz
Logical "1" Setup Time = 8.0 ns
Logical "0" Setup Time = 8.0 ns
Logical "1" and "0" Hold Times = 0 ns
 $t_{pd} \text{ "1"} = 12 \text{ ns}$
 $t_{pd} \text{ "0"} = 12 \text{ ns}$



1/2 OF DEVICE SHOWN

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



@
Test
Temperature
0°C
+25°C
+75°C

TEST CURRENT/VOLTAGE VALUES													P ₁ *	Gnd
mA					Volts									
I _{OL}	I _{OH}	I _{in}	2I _{in}	I _D	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}			
23	-2.0	-	-	-	0.4	2.5	4.0	-	5.0	4.5	5.5			
23	-2.0	1.0	2.0	-10	0.4	2.5	4.0	7.0	5.0	4.5	5.5			
23	-2.0	-	-	-	0.4	2.5	4.0	-	5.0	4.5	5.5			
TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:														
I _{OL}	I _{OH}	I _{in}	2I _{in}	I _D	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}			
-	-	-	-	-	2	-	1,4	-	-	-	14	-		
-	-	-	-	-	3	-	1,4	-	-	-	14	-	2,5,7,13	
-	-	-	-	-	4	-	1,2	-	-	-	14	-	3,7,13	
-	-	-	-	-	1	-	2,3	-	-	-	14	4	7,13	
-	-	-	-	-	1	-	2,3,4	-	-	-	14	5	7,13	
-	-	-	-	-	-	2	3	-	-	-	14	-	1,4,7,13	
-	-	-	-	-	-	3	2	-	-	-	14	-	1,4,7,13	
-	-	-	-	-	-	4	3	-	-	-	14	-	1,2,7,13	
-	-	-	-	-	-	1	-	-	-	-	14	-	2,3,4,7,13	
-	-	2	-	-	-	-	-	-	-	-	14	-	1,4,7,13	
-	-	3	-	-	-	-	-	-	-	-	-	-	1,4,7,13	
-	-	-	4	-	-	-	-	-	-	-	-	-	1,2,7,13	
-	-	-	1	-	-	-	-	-	-	-	↓	-	2,3,4,7,13	
-	-	-	-	2	-	-	-	-	-	-	14	-	7,13	
-	-	-	-	3	-	-	-	-	-	-	↓	-	↓	
-	-	-	-	4	-	-	-	-	-	-	-	-	-	
-	-	-	-	1	-	-	-	-	-	-	↓	-	↓	
5	-	-	-	-	-	-	-	-	-	-	14	5	1,7,13	
6	-	-	-	-	4	-	-	-	-	-	14	4	1,7,13	
-	5	-	-	-	4	-	-	-	-	14	-	4	7	
-	6	-	-	-	-	-	4	-	-	14	-	5	1,7,13	
-	-	-	-	-	-	-	-	-	14	-	-	-	4,5,7,13	
-	-	-	-	-	-	-	-	14	-	-	-	-	4,7,10	
-	-	-	-	-	-	-	-	-	14	-	-	-	4,7,10	

* Momentarily ground pin prior to taking measurement. (If pin is also in another column the pin must be returned to that voltage or current for measurement.)

MC3062 (continued)

OPERATING CHARACTERISTICS

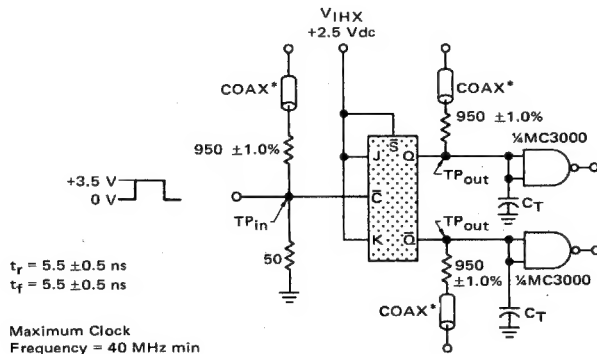
The data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

The flip-flop is set to the Q = 1 state by applying a low level to the $\overline{\text{SET}}$ input. The direct $\overline{\text{SET}}$ inputs may be used at any time without regard to the clock state. If these inputs are not used they should be returned to a voltage between 2.0 and 5.5 Vdc.

Negative edge triggering – The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low.

Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.

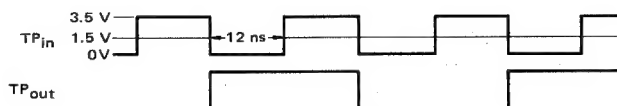
MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

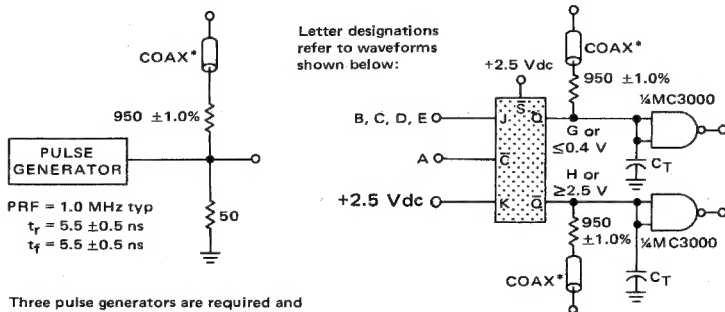
VOLTAGE WAVEFORMS AND DEFINITIONS



OPERATING CHARACTERISTICS (continued)

SWITCHING TIME TEST CIRCUIT

(For J Inputs; to test other inputs, refer to Test Procedures Chart)

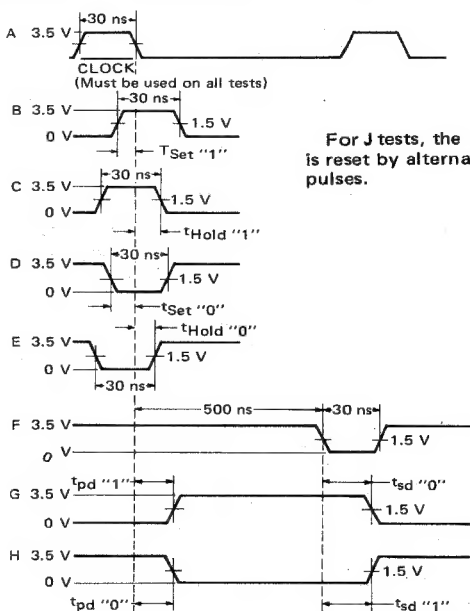


Three pulse generators are required and must be slaved together to provide the waveforms shown.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



For J tests, the flip-flop is reset by alternate clock pulses.

TEST PROCEDURES CHART

TEST	INPUT				Q*	Q̄*	LIMITS (ns)
	J*	SET*	K*				
tSet "1"	J	B	2.5 V	2.5 V	G	H	15
tHold "1"	J	C	2.5 V	2.5 V	G	H	0**
tSet "0"	J	D	2.5 V	2.5 V	≤ 0.4 V	≥ 2.5 V	15
tHold "0"	J	E	2.5 V	2.5 V	≤ 0.4 V	≥ 2.5 V	0**
tSet "1"	K	Gnd	F	B	H	G	15
tHold "1"	K	Gnd	F	C	H	G	0**
tSet "0"	K	Gnd	F	D	≥ 2.5 V	≤ 0.4 V	15
tHold "0"	K	Gnd	F	E	≥ 2.5 V	≤ 0.4 V	0**
tpd "1"	Delay from CLOCK to Q during tSet "1" J test. Delay from CLOCK to Q̄ during tSet "1" K test.						18
tpd "0"	Delay from CLOCK to Q̄ during tSet "1" J test. Delay from CLOCK to Q during tSet "1" K test.						18
tsd "1"	Delay from SET to Q during tSet "1" K test.						18
tsd "0"	Delay from SET to Q̄ during tSet "1" K test.						18

*Letters shown in test columns refer to waveforms shown at the left.

**t_{hold} is typically a negative number.